Design and Implementation of a 2.62 uW Low-power Baseband Processor for Passive UHF RFID Tags

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Abstract—In this paper, an ultra-low-power baseband processor for a UHF Passive RFID Tag is presented. It proposes a prominent RFID tag baseband architecture which is compliant with the ISO18000-6B UHF RFID protocol. Several low-power design approaches are employed to reduce the power consumption, including low voltage low operation frequency approach, clock gating technique, clock strobe design, asynchronous operating scheme and optimal power management. The chip has been designed and fabricated successfully in TSMC 0.18um CMOS Mixed Signal Process. Power analysis shows that the baseband processor consumes 2.62uW at 1V supply voltage when it is inventoried by the reader.

***Keywords*—UHF, RFID, Baseband, Low-power, Tag**

I. INTRODUCTION

RFID (Radio-Frequency Identification) has been widely used in the past few years with a great deal of significant features in technology and applications. It has been applied in many areas, including access control, transportation payment, automatic highway toll, product tracing as well as postal logistics[1]etc. Because of relatively large communication range, and lower cost in comparison to microwave or active tag [2], UHF Passive Tag is becoming the most promising technique for RFID applications.

The main objective in designing UHF passive RFID tag is to maximize the operating range, which depends on the rectifier efficiency and power consumption of tag. In addition, modulation impedance when transmitting data to reader should also be considered for less mismatch of the power matching network [2]. Studies about high-efficiency rectifier which convert the received RF input signal energy to DC supply voltage [3][4]and development on low-power consumption of RF/Analog Front-end[5][6] have been reported frequently in recent years. However, novel low power baseband processor design is rarely reached [7][8][9],which falls far behind the power consideration of digital section of 1uW for long range tag design. Due to its complexity, the baseband processor accounts for a large proportion of the whole power consumption. Therefore the extremely low-power design of baseband processor is becoming increasingly critical.

The baseband processor plays a great role – Central Control Unit. It is responsible for decoding Manchester data, performing CRC checking and computing, command analyzing, power management, state transition controlling and encoding returning data. The baseband also controls the analog front-end for saving power, especially switches on/off the backscatter modulating section. In general, the baseband should be able to contribute to reducing the power consumption of the overall chip.

This paper proposes a promising RFID tag baseband architecture. Together with its asynchronous operating scheme and corresponding power management, the tag can achieve a very low order magnitude of power consumption while fulfilling completely the ISO18000-6B protocol. Because of lower forward link and return link frequency and lower complexity compared with ISO 18000-6C or EPC C1G2 protocol, the baseband processor can be much simpler and consumes much lower power, therefore can be used in longer-range application.

This paper is organized as follows. Section II proposes a novel low-power baseband architecture and its asynchronous operating scheme. In Section III some advanced low-power approaches adopted in the design are explained. Section IV describes the ASIC implementation and FPGA prototyping verification of the digital core. Section V shows the simulation performance and measurement results. Finally the conclusions are presented in section VI.

II. PROPOSED ARCHITECTURE AND ASYNCHRONOUS OPERATING SCHEME

Fig 2 shows the proposed architecture of the system .The system consists of 12 modules: Manchester decoder (DEC), cyclic redundancy check (CRC), serial to parallel (SPC), output control unit (OCU), fm0 encoder (ENC), random number generator (RNG), collision arbitration counter (CNT), quiet timer (TMR), system clock generator (SCG), reset signal generator (RSG), memory access control (MAC) and finite state machine (FSM). Each module performs as a single function module and allows deactivated whenever unused.

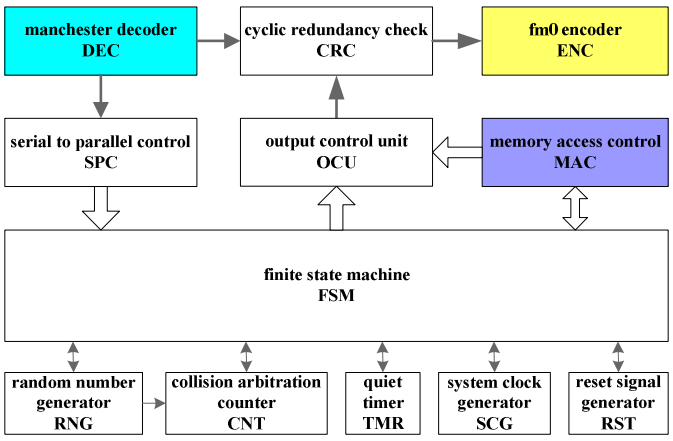


Figure 1. Proposed architecture of baseband processor

The asynchronous operating scheme is explained as follows: On receiving signal from the interrogator (RX working state), the Manchester decoder detects and decodes

the incoming demodulated data and wakes up the FSM. The FSM enables the CRC and SPC to perform cyclic redundancy check and serial-to-parallel operation simultaneously and will not disable them until the data receiving is completed. Depending on different receiving command, FSM shall reset, increment or decrement the collision arbitration counter and employs relevant operation (PROCESS working state). Thereafter, the FSM waits for the TMR timeout and then enables OCU to access data from the nonvolatile memory and sends it to encoder serially. The encoder performs fm0 coding and data formatting on the serial data and sends it to RF/analog front-end (TX working state). After the encoding is finished the FSM can disable these modules and then performs state transition of the tag. Subsequently, The FSM disables itself immediately and enables the decoder, waits for another incoming data and hence to be waked up (IDDLE working state). Each peripheral module communicates with FSM through shake-hand signals to make sure the disabling and enabling operation under certain conditions works correctly.

The advantage of this asynchronous operating scheme is that it can achieve a very low-power design. In the asynchronous scheme, each module is activated whenever needed and remains deactivated otherwise. Later the baseband processor can be performed power management effectively and clock gating technique on all modules including FSM automatically.

III. LOW-POWER DESIGN APPROACHES

There are two main components of power consumption in digital CMOS circuit, namely the static power and the dynamic power. The dynamic power dissipation P_{dyn} is caused by the charging and discharging of parasitic capacitances in the circuit while the main causes of static (leakage) power are subthreshold leakage, gate leakage and so on, which are beyond the scope of our discussion in this paper. In Deep sub-micron Technology, the dynamic power is the dominant power consumption. Our focus is on saving the dynamic power.

According to [10], the dynamic power consumption is given by the golden formula:

$$P_{dyn} = C_L \cdot {V_{dd}}^2 \cdot \alpha \cdot f \tag{1}$$

Where C_L is the load capacitance, V_{dd} is supply voltage, α is the switching activity and f represents the clock frequency.

A. low voltage and low operating frequency approach

The dynamic power consumption of a synchronous design is directly proportional to its clock frequency. Consequently, selecting the clock frequency is a key decision for power reduction. The lower the clock frequency is, the lower the power consumption will be.

However, there is a minimum clock frequency imposed by the requirements of the protocol. In this case, the clock frequency has to be high enough to decode the incoming data and to backscatter the response in each specified data rates. Besides, the circuit delay depending on the clock frequency should be short enough to satisfy the tag response time requirement. Fortunately, this is not critically required by the specification.

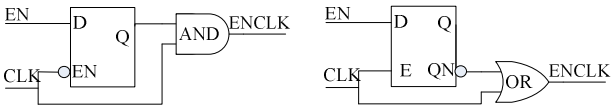
As specified in the protocol, the forward link frequency is defined as 40kbps, and the backward link frequency (BLF) is 40kbps or 160kbps depending on the delimiter field in the forward link data frame. The backscattered signal is encoded as FM0. Taking into account that the coding requires a transition in the middle of the transfer symbol, it is necessary to have a clock of at least the double frequency of BLF. Moreover, a double frequency is high enough to decode the forward link data and to fulfill all the specification in the protocol, therefore the clock frequency is chosen as follows:

$$f_{clk} = 2 \cdot BLF = 320kHz \tag{2}$$

Since the dynamic power dissipation is proportional to the square of operating voltage and static power dissipation is also proportional linearly to the operating voltage, a low operating voltage could reduce the power consumption in an effective way. In the present work, we selected a 0.18um CMOS process with low supply voltage of 1.0V, in order to obtain a lower extremely power consumption and attain a relatively lower cost.

B. clock gating technique

Clock gating is a dynamic power reduction method in which the clock signals are stopped for selected register banks during times when the stored logic values are not changing. Shutting off the clocks eliminates unnecessary switching activity that would otherwise occur to reload the registers on each clock cycle. In our design, we employ this clock gating method at both module level and register level. The clock gating circuit is shown in Fig.2.



A B

Figure 2. Positive gating logic(A) and negative gating logic(B)

Module level clock gating involves shutting off the entire module in the design. Since each module in the design is used only for a specific mode of operation (e.g., the decoder and encoder in the architecture may not be active at the same time). The encoder can be shut off during data receiving stages or vice versa. Module level clock gating is performed by power management which saves a large amount of power. The gate clock circuit is shown in fig 4 and should be incorporated into the RTL code by the designer.

In order to reduce even more power consumption, the register level clock gating is applied, which involves gating the clock to a single register or a register bank. However, gating a single bit of register costs an extra associated penalty of power consumption in the clock gating logic. To decide if a register bank is large enough to be clock gated we have to analyze the switching activity and the dynamic power of the bank.

However, the synthesizing tool can optimize the registers to be gated and then inserts the clock gating automatically.

C. *clock strobe design*

To implement different backward link frequency, we have to use different division clock. However, an additional clock will increase the complexity and decrease the reliability of the whole system. Extra clock also needs more considerations in the CTS flow, with increased power consumption in the clock network. We apply a new method called clock strobe design, with which the frequency division clock will be only used as a clock enabling signal for data sampling. Consequently, register level clock gating can be performed. The detailed illustration is shown in Fig.3.

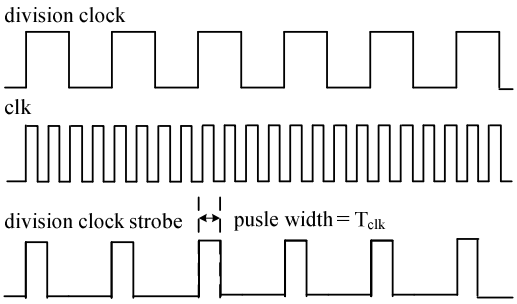


Figure 3. Clock strobe design

When using this method we need to consider and tradeoff the power saving by the simplifier clock network against the power saving by a lower frequency clock domain design. However, in our design, the encoder module which could use a lower clock frequency is not big enough to increase an additional clock domain.

D. *Power management*

Based on the asynchronous operating scheme, an efficient power management scheme can be performed. To employ power management, four working states have been defined previously. In each state, only several modules need to be active while the rest are deactivated during the execution of operations. Table I shows the relationship between the working states and major modules.

TABLE I. WORKING STATES OF THE BASEBAND PROCESSOR

MODULE	WORKING STATE			
	IDDLE	*RX*	*PROCES*	*TX*
DEC	ON	ON	OFF	OFF
SPC	OFF	ON	OFF	OFF
CRC	OFF	ON	OFF	ON
OCU	OFF	OFF	OFF	ON
ENC	OFF	OFF	OFF	ON
MAC	OFF	ON	OFF	ON
CNT	OFF	OFF	ON	OFF
TMR	OFF	OFF	ON	OFF
FSM	OFF	ON	ON	ON

To ensure the system works properly, the SCG, RST and RNG are always active through all the working states hence are not listed in the table. However, the power consumption of these modules is not comparable to the whole power consumption. Furthermore, module level clock gating inserting is adopted referring to Tab.1.

IV. IMPLEMENTATION AND VERIFICATION

The RFID baseband processor has been described in verilog language and synthesized with Synopsys Design Compiler. Layout operations have been performed with Cadence Encounter. Also, commercial verification-flow is employed. Finally, the digital baseband processor is fabricated successfully in TSMC 0.18um CMOS Mixed Signal Process. The overall area of ISO18000-6B baseband circuit is 52094 um^2, which consumes 5933 equivalent gates. Fig.4 shows the photomicrograph of the developed chip.

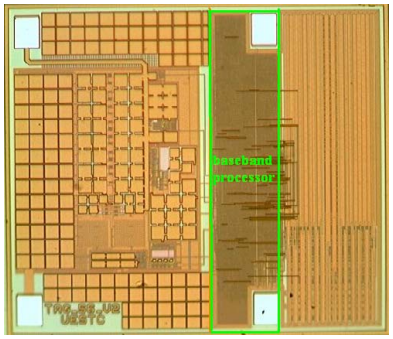


Figure 4. Photomicrograph of the developed chip

In order to verify our design functionally, we implement the design in the Xilinx Virtex-II Pro XC2VP30 FPGA and apply real-time verification. A commercial reader and a board-level demodulator/ modulator are used to construct the verification platform. The demodulator demodulates the signal from the commercial reader and then generates all necessary input vectors provided to the FPGA based digital processor. Once any output data is backscattered by the processor, it is sent to the modulator and received by the reader. The demodulator/modulator and the FPGA based digital processor system act as a complete tag with the help of several required DC power supplies. The whole verification platform also acts as a complete RFID system. To verify the communication protocol and collision arbitration algorithm, we can simply send different commands with different payload through the reader and check the response of the digital processor. Furthermore, an embedded online Logic Analyzer provided by Xilinx FPGA is used to study the internal signal processing of the baseband processor.

To reduce the error rate of the digital processor, we also generate all random input output test vectors on the basis of the protocol and program them into the random access memory (RAM) of the Xilinx FPGA. By comparing the output vector of the digital processor and the output test vectors automatically [11], we can improve the error coverage percentage. Consequently, through the use of these two verification methods, the functionality of the design could be verified.

V. SIMULATION AND MEASUREMENT RESULTS

To achieve the power consumption of the digital baseband processor, several simulations have been carried out. Synopsys Power Compiler has been exploited for average power consumption estimation, which shows that the digital processor consumes an average power of 3.084uW over the whole possible operation including read and write mode.

A more effective method is to use instantaneous power analysis, with which we can gain the real-time power consumption under different input test vectors. Using Synopsys Nanosim simulation tool, we can attain the instantaneous current of each node in the circuit. Fig.5 shows the functional simulation and corresponding power consumption of the whole digital processor.

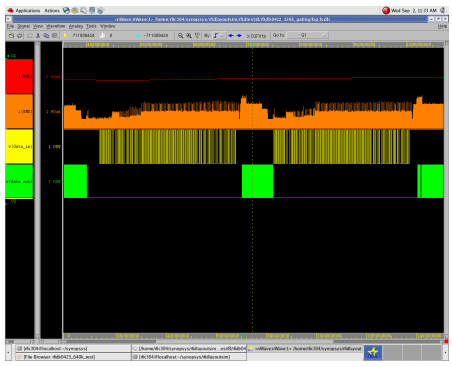


Figure 5. Simulation results of nanosim

As shown in Fig.5, the instantaneous current of the GND node of the digital processor is 2.62uA when the tag is inventoried by the reader. At 1V supply voltage, its corresponding power consumption is 2.62uW.

The fabricated chip has been tested under stringent ESD protection. Measurement result shows that the digital processor fulfills the ISO18000-6B protocol and consumes a current of 3.89uA at 1V supply voltage including IO pads, where the current is measured by FLUCK 289 TRUE RMS MULTIMETER which has a DC current accuracy of 0.15%. Simulation and measurement result confirm the validity of the proposed design and exhibit a remarkable performance on low-power consumption.

VI. CONCLUSION

In this paper, an ultra-low-power baseband processor for a UHF Passive RFID Tag has been introduced. High performance has been achieved by means of careful system design and several low power strategies. Also, new verification methods are performed to ensure the tag works well in any case. The tag can achieve a very low order of power consumption while fulfilling completely the ISO18000-6B protocol. Simulation Results shows that a total power dissipation of 2.62uW at 1V supply voltage is reached when it is inventoried by the reader. Due to its lower complexity, the overall area of this baseband circuit is only 52094 um^2 estimated by the Design Compiler.

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