Design of Folded-cascode UWB Low Noise Amplifier with Low Power Consumption

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Abstract— In this paper, we proposed a low noise amplifier (LNA) for ultra wideband (UWB) application using TSMC 0.18µm CMOS technology. To satisfy the wide input matching, LC high-pass filter matching network is utilized in the first stage. To obtain the low power characteristic, folded-cascode with current reused technique is utilized in the second stage. The designed UWB LNA has the voltage gain of 17.6 ~ 19.7 dB and the noise figure of 1.8 ~2.2 dB over the frequency band of interest (3.1-10.6 GHz). The total power consumption of the UWB LNA is 4.0 mW (core 2.93 mW) from 1 V supply voltage.

***Keywords* — Low Noise Amplifier, Folded-cascode, Current – reused technique, Low power consumption, Ultra wideband**

I. INTRODUCTION

In recent years, Ultra wideband(UWB) systems have attracted much interest due to their capability of transmitting data with high data rate and low power consumption [1]. In the IEEE 802.15.3a standard, UWB systems are allocated for use of frequency band from 3.1 to 10.6GHz. In the UWB receiver systems, one of the most critical devices is a low noise amplifier (LNA) because the noise figure (NF) is dominant in the first stage of the receiver. It must satisfy the low NF, sufficient gain with flatness over the wide frequency range. Additional requirements such as high integration, low power consumption and low cost are demanded [2].

Several CMOS LNAs have been reported for UWB receiver systems [3]. Including current-reused technique. Current reused technique can be classified into two types. One is made of NMOS and PMOS pairs in shunt configuration to achieve current reuse. This technique increases the overall effective transconductance with same power consumption [4]. However, it can cause linearity problem because of the different mobility of NMOS and PMOS transistors. Another is the current reused topology utilizing the two stage cascade to share the same current source.

In this paper, we propose a low power, high gain UWB LNA using TSMC 0.18µm RF CMOS technology. The proposed UWB LNA has two stages. To satisfy the wide input impedance matching, high–pass filter (HPF) are utilized in the first stage. Using the folded-cascode topology with current reused technique in the second stage, low power consumption and sufficient voltage gain requirement can be achieved.

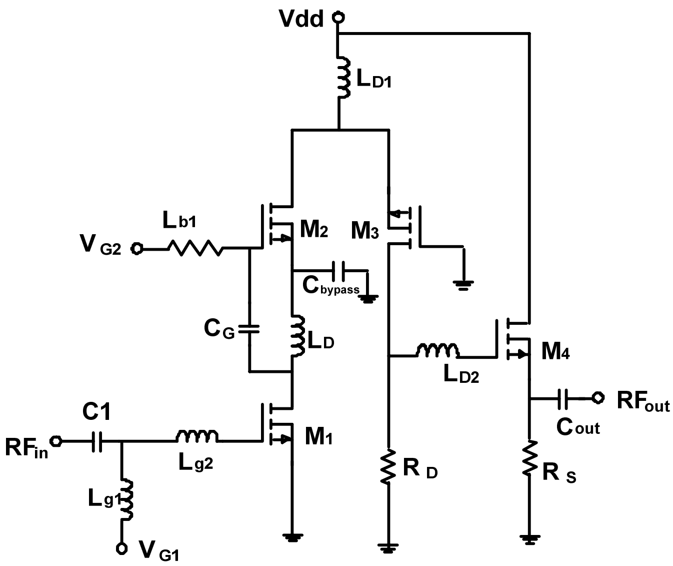


Figure 1. The complete schematic of the the proposed UWB LNA

II. LNA CIRCUIT DESIGN

Fig. 1 shows a complete schematic of the proposed UWB LNA. A simple high pass filter (HPF) type matching network is adopted in an input stage to obtain the impedance matching over the entire frequency band. As shown in Fig. 2, passband characteristics over the entire UWB band can be achieved by combining HPF (L_{g1}, C_1) and low pass filter (L_{g2}, C_{gs}). Fig 3. shows the simulated S_{11} characteristics with HPF and without HPF.

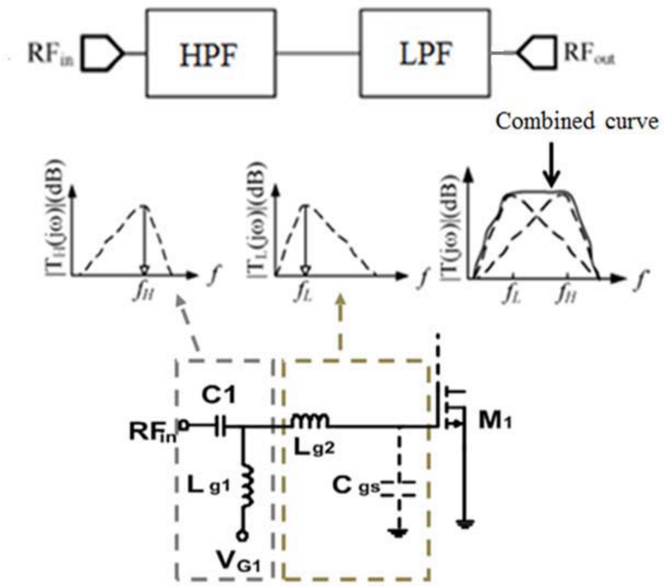


Figure 2. Formation of the passband characteristic using LC filters

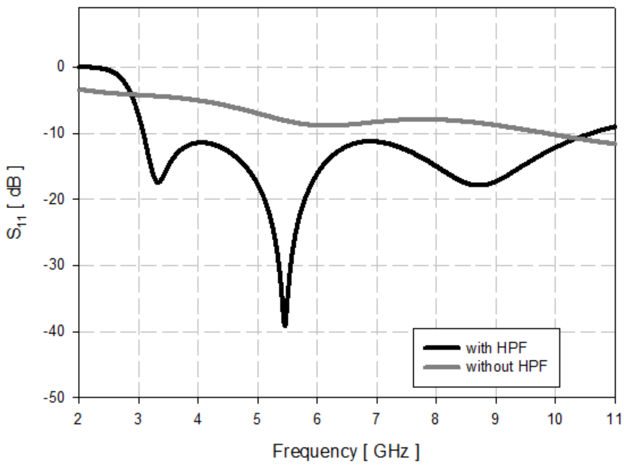
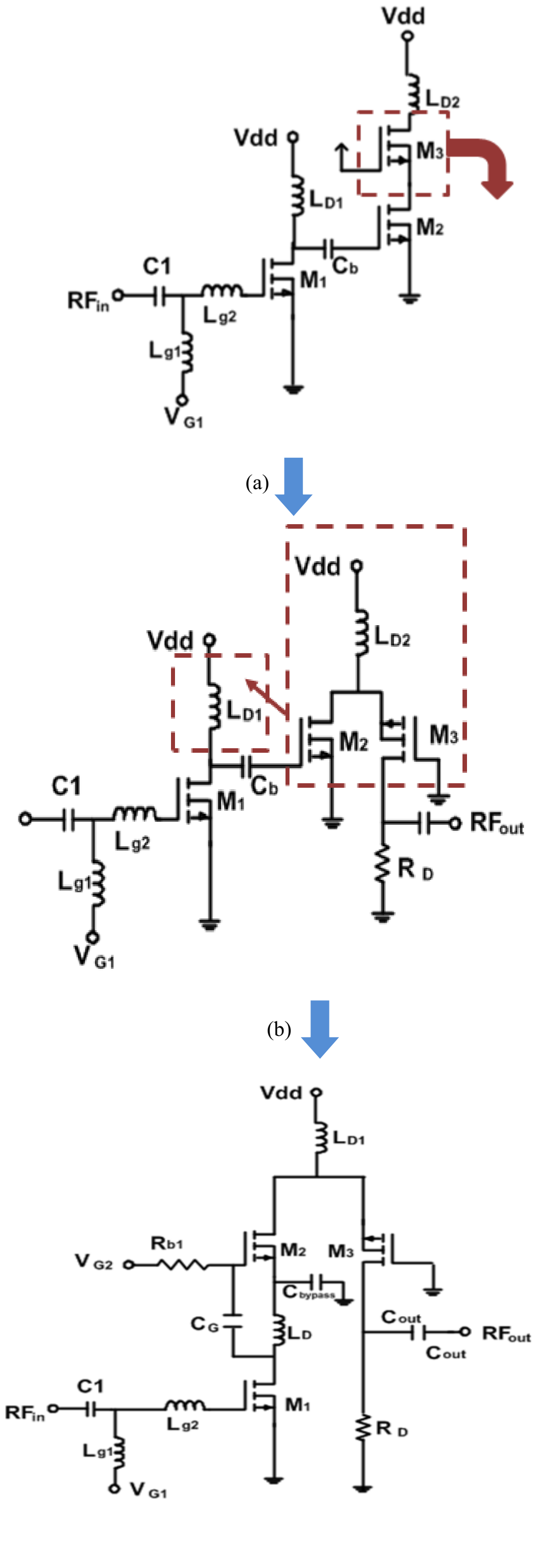


Figure 3. S_{11} characteristics between with and without HPF

The folded-cascode topology is adopted in the second stage to satisfy the low power consumption [5]-[6]. Conventional cascade topology requires a large supply voltage because of stacking a large number of transistors [7]-[8]. To avoid this problem, one can use a PMOS transistor instead of NMOS transistor (M3), as shown in Fig. 4(b). To reduce the power consumption further and to obtain the sufficient gain, a current reuse technique is usually adopted [9]. By utilizing current reuse technique, a two-stage topology shown in Fig. 4(b) can be converted to the current reuse topology shown in Fig. 4(c). By stacking folded–cascode stage on the top of the common-source(CS) amplifier, the total transconductance is increased with the same current consumption. C_G, L_D, C_{bypass} are coupling capacitor, RF choke and capacitor providing AC ground, respectively.



(c)

Figure 4. The propodse UWB LNA utilizing folded-cascode with current reused technique (a) A two-stage cascade topology with conventional cascode (b) A two-stage cascade with folded-cascode topology (c) folded-cascode topology with current reuse technque

The flat gain over the entire bandwidth is an important factor of UWB LNA. Peaking inductor L_{D2} is inserted between the core stage and output buffer to extend the 3-dB bandwidth and adjust the flat gain at high frequencies. Fig.5 shows the simulated S_{21} response of the proposed UWB LNA for various values of L_{D2}. Output buffer is a source follower which provides 50Ω wideband output impedance matching. The optimum values of all the components are listed in Table 1.

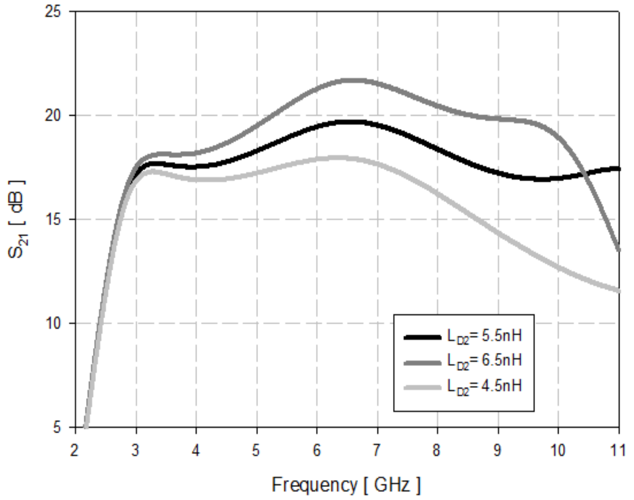


TABLE 1. CIRCUIT PARAMETER VALUES

M1	100 / 0.18µm	C_G	1.5 pF
M2	84 / 0.18µm	C_{bypass}	3 pF
M3	76 / 0.18µm	R_{b1}	1.5 Ω
M4	40 / 0.18µm	L_{D1}	1.7 nH
C_1	0.6 pF	L_{D2}	5 nH
L_{g1}	2.7 nH	R_D	1.5 Ω
L_{g2}	1.8 nH	R_S	300 Ω
L_D	12.5 nH	C_{out}	2.2 pF

Figure 5. S_{21} response of the proposed UWB LNA for various L_{D2} values

III. SIMULATED RESULT

The proposed UWB LNA was designed using TSMC 0.18 µm CMOS technology. Fig. 6 shows the simulated S-parameters of the designed UWB LNA. 10 dB return loss bandwidth is enough to cover the frequency band from 3.1 GHz to 10.6 GHz. The simulated voltage gain ranges from 17.6dB to 19.7dB over the whole UWB frequency band. The stability factor is calculated by using the simulated S-parameters and its value is larger than 1 across the entire bandwidth. The simulated NF ranges from 1.8 dB to 2.2 dB over the desired frequency band. The input-referred 1-dB compression point (P1dB) is -15.3 dBm and input-referred third-order intermodulation point (IIP3) is -5.31 dBm at 6 GHz as shown in Fig. 7. The total power consumption of the proposed UWB LNA is 4.0 mW(core 2.93 mW). Performance summary of the designed UWB LNA is listed in Table 2 and compared with previously reported CMOS UWB LNAs .

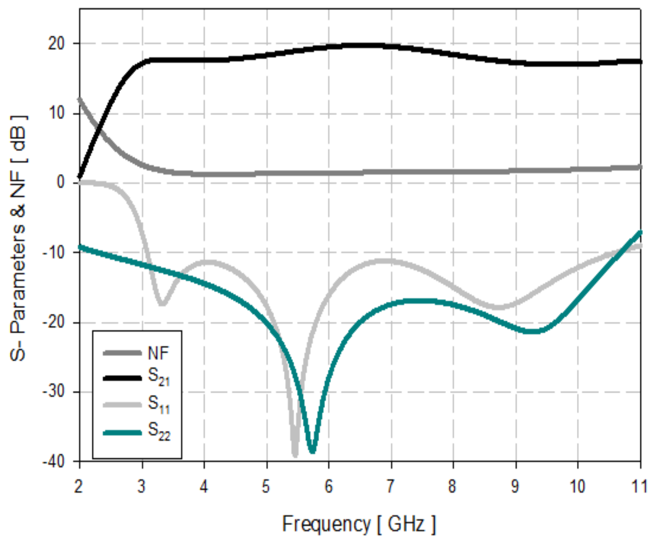


Figure 6. Simulated S-Parameters of the proposed UWB LNA

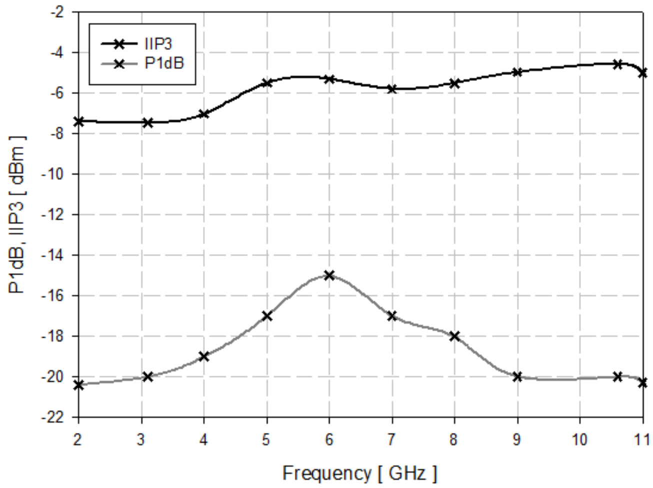


Figure 7. Simulated IIP3 and PIdB of the proposed UWB

IV. CONCLUSION

In this paper, we proposed a low power, high gain UWB LNA. To satisfy the wide input impedance matching, high–pass filter (HPF) are utilized in the first stage. Using the folded-cascode topology with current reuse technique in the second stage, low power consumption and sufficient voltage gain requirement can be achieved. The designed UWB LNA has better ratio of the gain to power consumption and noise figure comparing to previous researches.

TABLE2. PERFORMANCE SUMMARY AND COMPARISON TO UWB CMOS LNA

Reference	Measured [10]	Measured [11]	Measured [12]	Simulated [13]	Simulated [14]	Simulated [15]	Simulated (This work)
Technology	0.18 µm RF CMOS	0.13 µm RF CMOS	0.13 µm RF CMOS	0.18 µm RF CMOS	0.18 µm RF CMOS	0.18 µm RF CMOS	0.18 µm RF CMOS
Bandwidth [GHz]	3.1-10.6	3.1-10.6	3.1-10.6	3-8	3-5	3.1-10.6	3.1-10.6
Supply voltage (V)	1.5	1.2	1.2	1.8	1.0	1.8	1.0
S_{11}, S_{22} [dB]	< -8	<-10	<-15	<-8	<-10.76	<-7.8	<-10
Gain [dB]	13.5-16	13.7-16.5	7.69-8.15	15.2	15.7-16.7	10	13.0-19.5
NF [dB]	3.1-6	2.1-2.8	2.5-4.56	3.14-6.8	2.6-2.89	1.75-2.2	1.8-2.21
IIP3 [dBm]	-7*	-7*	-4*	-6.63*	-8^	-	-5.31*
Power [mW]	11.9	9.0	10.68	$9.5^{\#}$	5.56	12	4.0 ($2.93^{\#}$)

* at 6GHz. ^ at 4GHz, $^{\#}$ core

V. ACKNOWLEDGMENT

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