

The optimized pre-processing algorithm for hardware design implementation

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Abstract— Stereo matching algorithm is used to get depth map image using the matching cost, the difference between left and right images, from stereo camera. To get accurate depth map image, image which will be used for stereo matching algorithm needs camera calibration procedure. High depth map image quality will be obtained, if accurate camera calibration is applied accurately. However, the conventional rectification circuit size will grow exponentially with high frame rate and high resolution images. To compensate for this part, we proposed the optimized pre-processing algorithm for hardware design implementation

Keywords— Depth-map, stereo camera, 3D, rectification, Stereo matching, disparity, scan-line

I. INTRODUCTION

3D stereo camera algorithm is used to get depth map information using disparity from two cameras.[1][2] But, it can't make the same stereo camera module even though using sophisticated machine in manufacture process. Therefore, in order to maintain the same shape of two cameras, calculate the parameters of each camera. Offsets are obtained from the left and right parameters respectively, it is used for left-right images placed on the same scan-line. This process is referred to as pre-processing or rectification. In other words, more accurate depth map in order to extract information,[3] the first pre-processing is required. Perform traditional rectification by applying the parameter values to reference table stored in ROM. If the system needs more higher frame rate, rectification circuit size is also dramatically increase. That is weak point of conventional rectification method.

In this paper, we newly suggest implemented method for reducing circuit size, low cost, compensating disadvantage of

conventional method. Proposed algorithm is separated four parts as address generator, data store, interpolator. Each part is explained as below.

A. stereo camera parameter generator

Structure of conventional method implemented using eight ROM is shown as Figure1.

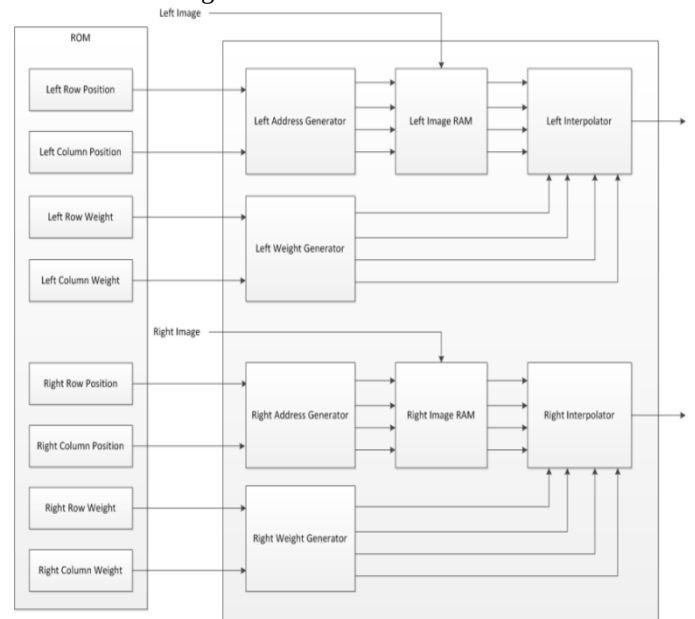


Figure 1. Conventional Hardware structure for rectification

It is used four ROM in left camera and the other four ROM used in right camera. In these ROM, is contained column information, row information, left weights value and right weights value. Each ROM has stored pixel address value, it can make from below equation.[4]

$$\begin{aligned} x &\leftarrow (u - c'_x)/f'_x \\ y &\leftarrow (v - c'_y)/f'_y \end{aligned} \quad (1)$$

$$[X Y W]^T \leftarrow R^{-1} * [x y 1]^T \quad (2)$$

$$x' \leftarrow X/W$$

$$y' \leftarrow Y/W \quad (3)$$

$$x'' \leftarrow x'(1 + k_1 r^2 + k_2 r^4 + k_3 r^6) + 2p_1 x' y' + p_2 (r^2 + 2x'^2)$$

$$y'' \leftarrow y'(1 + k_1 r^2 + k_2 r^4 + k_3 r^6) + p_1 (r^2 + 2y'^2) + 2p_2 x' y' \quad (4)$$

$$\text{map}_x(u, v) \leftarrow x'' f_x + c_x$$

$$\text{map}_y(u, v) \leftarrow y'' f_y + c_y \quad (5)$$

Equation(5) is final equation about generating left coordinates and right coordinates. In this case, matrix of original camera equation is equation(6). f_x is original scale factor of x axis, f_y is original scale factor of y axis, c_x is original principal point of x axis, c_y is original principal point of y axis.

$$A = \begin{bmatrix} f_x & 0 & c_x \\ 0 & f_y & c_y \\ 0 & 0 & 1 \end{bmatrix} \quad (6)$$

$$A' = \begin{bmatrix} f'_x & 0 & c'_x \\ 0 & f'_y & c'_y \\ 0 & 0 & 1 \end{bmatrix} \quad (7)$$

In addition, generating matrix of new camera is A' , f'_x is new scale factor of x axis, f'_y is new scale factor of y axis, c'_x is new principal point of x axis, c'_y is new principal point of y axis. If size of image is $N \times M$, u is $(1 \sim N)$ index of x axis and v is $(1 \sim M)$ index of y axis. Role of address generator is performed calculation of equation at the above for making the new address of pixel data instead of original pixel data address $(1,1)$ to (N, M) . Also, k_1, k_2, p_1 and p_2 are distortion variable.

For using interpolation process, weight value is generated by left column weight ROM, left row weight ROM, right column weight ROM and right row weight ROM. Likewise, generating left-right address and left-right weight are used for interpolator. Interpolator get these values for making rectified image.

However, pre-module block is huge size containing eight ROM like as conventional rectification method. Thus, the frame size including many data, it is implemented using only four ROM and implemented to real-time processing by using the equivalent circuit and the circuit size is reduced significantly. Address generating unit in real time, a new pixel that matches the incoming video in real time, that generates the address block. Generating unit a total of four kinds of address information to provide real-time, left column location, left row location, and right column, right row position where the left and right cameras respectively, are provided.

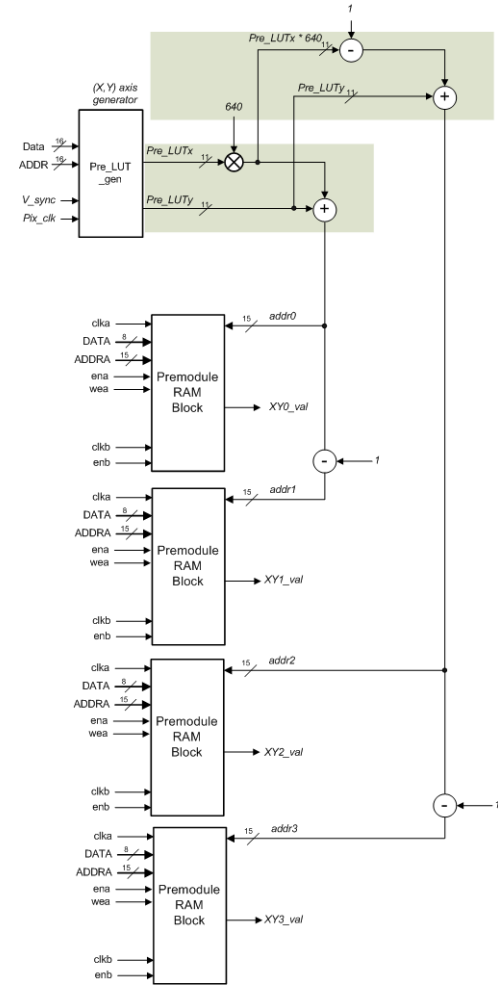


Figure 2. Newly proposed structure of rectification for 3D stereo camera.

first of all, original equation can be changed to the equivalent equation approximately when R^{-1} is identity matrix. Thus, we assume $R^{-1} = I$ (I is the identity matrix), the divider is not required to perform the operation. Also, circuit is more smaller and reducing delay and we can ignore the r^6 value in equation because, r^6 value is very small floating point value. It is characteristic of stereo camera. In fact, when the fixed point math to do, close to zero, a very small point in the hardware does not cause significant performance degradation. Therefore, Hardware is applied to equivalent optimized equation for reducing the complexity of the circuit cost and maintaining performance.

B. RAM model design

RAM structure is divided into two parts, the first part is the write address generation block and the second part is the read address block. That structure is called pre_LUT_gen. Write address block is performed the write process sequentially. left and right camera are composed of four RAM respectively for interpolation process. Each RAM has the same of writing

address. But, all of read address are different, those read address is shown as below.

$$\begin{aligned}\text{addrb0} &= (\text{LUTx mod } 30) * 640 + \text{LUTy} \\ \text{addrb1} &= \text{addrb0} - 1 \\ \text{addrb2} &= ((\text{LUTx} - 1) \text{ mod } 30) * 640 + \text{LUTy} \\ \text{addrb3} &= \text{addrb2} - 1\end{aligned}$$

In case of 640x480 pixel size, eight RAM (4 left RAM and 4 right RAM) are composed 8 bit input and 19200 depth, totally, four kinds of read address do modular calculation and get the up, down, right, left pixel value, each values has 1 pixel gap, it is use for interpolation process.

C. interpolator design

Conventional interpolation method uses the weight ROM, each ROM are stored weight value to left and right ROM respectively for interpolation process.[5] x axis value and y axis value are multiplied with this weight values respectively. After multiplication, all of multiplied values are summing. After summing, interpolation value is divided total sum value into 4. Newly proposed method is reduced the computational burden and remove the weight ROM, Hardware complexity is decrease about half and maintaining performance of conventional method.

D. rectification results

Both of conventional method and proposed method is implemented by FPGA based on VHDL language. We can test and confirm the output image from model simulator.

Figure 3 shows the image of rectification that is implemented by ROM using conventional equation.



Figure 3. Rectification scene using conventional structure based on 3D sensing stereo camera.

Figure 4 shows the image of rectification that is implemented by RAM using suggested equivalent equation.



Figure 4. Rectification scene using Newly proposed structure based on 3D sensing stereo camera.

From a results, two images on the same scan line position to the same object can be found.

II. CONCLUSIONS

3D stereo camera algorithm is used to get depth map information using disparity from two cameras. But size of rectification circuit depend on frame rate.[7][8] To overcome this problem, we newly proposed rectification algorithm based real time processing using RAM. We are modified equivalent equation instead of conventional equation for reducing computational burden and also, we can use RAM for real time rectification process and system is composed only 4 RAM instead of 8 ROM in original method that is expected to low cost and smaller size. pre-module is designed using FPGA that is implemented by Xilinx virtex5. it is designed based on real time processing and it is implemented using VHDL language. To comparison performance of rectification, we use Model simulation tool as Modelsim software. As a result, in case of general method, all of the blocks are designed ROM based that is huge size. On the other hand, case of proposed optimization method is smaller and same performance comparing with general method.

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