Sampling Jitter Mitigation with a Cascade Multiplier for Direct RF Bandpass Sampling Receiver

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Abstract— **The sampling jitter is one of the main problems in the direct RF bandpass sampling receiver architecture. Sampling jitter will seriously degrade the performance of the receiver, which can be improved effectively by digital compensation algorithm. This paper investigates the sampling jittering mitigation for the direct RF bandpass sampling receiver. Under the direct RF bandpass sampling receiver architecture, an approximate sampling jitter model is derived. From the model, it is noted that the adverse impact of the sampling jitter is presented as the phase noise component of the carrier. As a result, a sampling jitter migration approach is developed to eliminate the phase noise. Specifically, the cascade multipliers is able to effectively migrate the sampling jitter. The proposed jitter mitigation method requires low complexity, and can be easily implemented by hardware. Moreover, it has many merits over the existing sampling jitter migration algorithms, including real-time sampling clock jitter elimination, flexible implementation to meet the specific performance requirements by selecting different level of cascaded sampling jitter migration structure. Several experiments have been conducted with 3GPP LTE type signals. The root-mean-square (RMS) and SNR are taken as the performance measurements. Experimental results show that the proposed sampling jitter migration method is able to remove the adverse effect of the sampling jitter with a comparable performance of existing techniques at much lower complexity.**

Keywords—**direct RF bandpass sampling, sampling jitter, jitter mitigation, phase noise, cascade multiplier**

I. INTRODUCTION

The trend of wireless communication systems has been to put the analog-to-digital converter (ADCs) as close as possible to the antenna, such as in the direct RF sampling (DRFS) architecture. In a traditional RF receiver, a front-end consists of multiple stages of analog front-end mixers, analog oscillators and other analog devices to process a single RF signal. It has been shown that DRFS architecture brings many advantages, including a minimal set of front-end components, small scale, low cost and high degree of reconfigurability, which might fulfill the demand of Software Defined Radio (SDR)[1].

However, there are still some issues in practical implementation of direct RF sampling receivers, which hindered its application especially in wireless terminal. The first constrain factor is the ADC in DRFS requires a large analog input bandwidth, since the sample and hold circuit inside the ADC must accommodate the RF carrier. The second problem is sampling jitter. Sampling jitter refers to the sampling clock in the high speed ADCs fluctuation randomly from normal sampling instants. With the increasing of RF frequency and high data rates, the timing jitter problem becomes one of the major factors significantly limiting the performance of the direct sampling systems. This is because the performance of the ADCs is constrained by the behaviors of the sampling clocking and sampling circuit. The inconsistent behaviors of the circuits cause the sampling clock jitter or aperture jitter, which introduce additional noise into the sampling system[2]. The effects of sampling jitter is produce new discrete components and frequency selective attenuation, which will has an adverse effect on the SNR of the ADCs and effective number of bits (ENOB), which would cause serious degradation on the transmission performance.

Taking certain compensation approaches to resist the reducing of the ENOB in ADCs is a one of the technique options, however, the additional comparators will increase the power consumption by a factor of four for every lost of accuracy[3].

The digital compensation technology to eliminate the adverse impact of the sampling jitter has attracted great attention recently. In [4, 5] the authors using phase noise mitigation techniques for OFDM systems. In [6], the authors proposed a jitter mitigation method for the SC-FDMA systems. In [7], the authors proposed a mitigation method for direct sampling radio system. In [3], the authors developed the Bayesian post-processing methods to alleviate the impairment of the sampling jitter.

In this paper, the sampling jitter mitigation technique for the direct RF bandpass sampling receiver is investigated. In our study, we first develop an method of jitter estimation ,then derive the sampling jitter model in RF bandpass sampling receiver and analyze the effect of jitter on the receiver system. The error term caused by the sampling jitter from the non-uniform output samples of the receiver has been derived and a compensation method is proposed to mitigate this adverse effect accordingly. Intensive experiments have been conducted to evaluate and compare the performance of the proposed compensation method over reference technique in [7].

This paper is organized as follows, in section II a brief introduction of direct sampling receiver is given. In section III, we develop an method of jitter estimation . In section IV, the

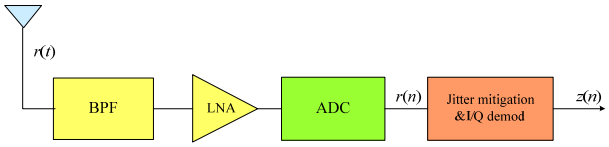

Figure 1. Direct RF sampling receiver

sampling jitter model of the direct RF bandpass sampling is presented. In section V, the state-of-the-art technology to mitigate the sampling jitter is developed. In section VI, the simulation experiments have been conducted and the performance analysis is given. Finally, section Ⅶ concluded our work.

II. Problem Formulation

The direct RF sampling receiver architecture is illustrated in Figure 1. It is noted that it employs an analog bandpass filter in front of the analog-to-digital converter to avoid sensitivity loss via aliasing of out-of-band noise and interfering signals. Then, the signal is put through the low noise amplifier (LNA) to adjust the dynamic range before the ADC sampling. ADC converts the analog signal to a digital signal. Thereafter, the down-conversion , sampling jitter removal, synchronization are carried in the digital domain for demodulation.

As it can be seen that the structure of the direct RF sampling receiver architecture removes bulky analog devices and greatly reduces the complexity and size of the whole system. It also improves the reconfigurability, especially when the accommodation of several standards on a single hardware platform is required.

III. Estimation of the Sampling Jitter

In order to mitigate the effects of sampling jitter, the sampling jitter of the system needs to be estimated first. Let $f(t)$ and $f(n)$ denote the analog signal and digital signal, respectively. In this section, we will first illustrate the method of estimating the sampling jitter in principle. And then a jitter parameter estimation algorithm termed as signal injection algorithm for direct RF bandpass receiver will be developed.

Let $r(t)$ be the analog output signal of the front end in a DRFS receiver. Taking a sinusoid frequency signal with frequency f_{ref} as a reference tone, which is injected before ADC sampling, the input signal of ADC $x(t)$ is denoted as

$$x(t) = r(t) + A\cos\left(2\pi f_{ref} t\right) \tag{1}$$

In ideal condition, ADC uniformly samples the input signal with the interval of T_s . However, in practice, due to the accuracy limitation of the clocking signal, the sampling jitter of ADC exists and denoted as ζ_n . It is reasonable to assume that the jitter is zero mean random variable.

Then, the output signal of ADC (named as the sampled signal) is given by

$$\begin{aligned} x(nT_s+\zeta_n) &= r(nT_s+\zeta_n) + A\cos\left[2\pi f_{ref}(nT_s+\zeta_n)\right] \\ &= r(nT_s+\zeta_n) + \frac{A}{2}\left(e^{j2\pi f_{ref}(nT_s+\zeta_n)} + e^{-j2\pi f_{ref}(nT_s+\zeta_n)}\right) \end{aligned} \tag{2}$$

In digital domain, the sampled signal is down-converted and subsequently filtered by a low-pass filter to isolate the jittered reference tone, which can be expressed as

$$y_n = LPF\left(x(nT_s+\zeta_n)\times e^{-j2\pi f_{ref} nT_s}\right) \simeq e^{j2\pi f_{ref}\zeta_n}/2 \tag{3}$$

Obviously, from (3), the jitter estimation can be implemented by [7]

$$\hat{\zeta}_n = \arg\{y_n\}/2\pi f_{ref} \tag{4}$$

It is noted that the operation of $\arg(\cdot)$ requires using the operation of $\tan^{-1}(\cdot)$ and asks higher implementation complexity and power consumption. To overcome this drawback, we propose a new jitter estimation algorithm (called signal injection algorithm) to estimate ζ_n , which is given as

$$\hat{\zeta}_n \approx \mathrm{Im}\{y_n\}/2\pi f_{ref} \tag{5}$$

IV. Jitter Model of Direct RF Bandpass Sampling Receiver

In general, the output signal of the front end in a DRFS receiver can be modelled as [8].

$$\begin{aligned} r(t) &= \mathrm{Re}\left\{(s_I(t) + js_Q(t))e^{j2\pi f_c t}\right\} \\ &= s_I(t)\cos\left[2\pi f_c t\right] - s_Q(t)\sin\left[2\pi f_c t\right] \end{aligned} \tag{6}$$

where $s_I(t) + js_Q(t)$ is the complex equivalent baseband signal corresponding to the received bandpass signal, f_c is the center frequency of the passband.

As illustrated in section Ⅲ, considering the jitter of ADC, the direct sampled signal with sampling frequency f_s can be modeled as

$$\begin{aligned} r(nT_s+\zeta_n) &= \mathrm{Re}\left\{(s_I(nT_s+\zeta_n) + js_Q(nT_s+\zeta_n))e^{j2\pi f_c(nT_s+\zeta_n)}\right\} \\ &= s_I(nT_s+\zeta_n)\cos[2\pi f_c nT_s + 2\pi f_c\zeta_n] \\ &\quad - s_Q(nT_s+\zeta_n)\sin[2\pi f_c nT_s + 2\pi f_c\zeta_n] \end{aligned} \tag{7}$$

Then applying digital I/Q down-conversion to move f_{IF} to the baseband and filter out the spectrum out of baseband, we get the baseband signal z_n as follows,

$$\begin{aligned} z_n &= LPF\left(r(nT_s+\zeta_n)\times e^{-j2\pi f_{IF} nT_s}\right) \\ &= \left(s_I(nT_s+\zeta_n) + js_Q(nT_s+\zeta_n)\right)e^{j2\pi f_c\zeta_n} \\ &= s(nT_s+\zeta_n)e^{j2\pi f_c\zeta_n} \end{aligned} \tag{8}$$

where f_{IF} denotes the center-frequency folded to the Nyquist band, and f_{IF} is defined as follows:

If $f_{ix}\left(\frac{f_c}{f_s/2}\right)$ is

$$\begin{cases} even, f_{IF} = rem\left(f_c, f_s\right) \\ odd, f_{IF} = f_s - rem\left(f_c, f_s\right) \end{cases} \quad (9)$$

where f_c is the sampling frequency, $f_{ix}(a)$ is the truncated portion of argument a, and $rem(a,b)$ is the remainder after division of a by b.

Now, if the jitter ζ_n is sufficiently small compared to T_s, the contribution of the sampling jitter on the composite modulating I and Q components is much lower than that on the carrier components, (8) can be further simplified as

$$z_n = s\left(nT_s + \zeta_n\right)e^{j2\pi f_c\zeta_n} \approx s\left(nT_s\right)e^{j2\pi f_c\zeta_n} \quad (10)$$

From (10), it is clear that the sampling jitter ζ_n presents at the time-varying phase component of the z_n. In direct bandpass sampling system, it induces phase modulation effect, which would give instantaneous randomly varying frequency offset to the equivalent baseband signal.

Therefore, from (10), it is clear that the undesired sampling jitter component can be eliminated by compensating the phase component directly. Carefully examining (10), we note that the compensation can be implemented by directly multiplying $e^{-j2\pi f_c\zeta_n}$ on z_n which is similar to the method proposed in [7], if the sampling jitter ζ_n is given. However, if doing so, we need to implement the complex exponential multiplier, which actually is difficult in hardware implementation at RF receiver. In order to lower down the computational cost in implementing the jitter compensation according to (10), a new jitter mitigation method in terms of cascade multiplier is proposed and is described in next section.

V. PROPOSED JITTER MITIGATION METHOD

In this section, an effective jitter migration method using multiplier cascade will be derived, which acts as a multistage compensation system to recover the uniform samples from the non-uniform sampled signal.

Essentially, our ultimate goal is to reconstruct the sampled signal $s\left(nT_s\right)$ from z_n in (10) without adverse effect of the sampling jitter in the digital domain.

By Taylor expansion on $e^{j2\pi f_c\zeta_n}$ in (10), we can derive the following

$$z_n \approx s\left(nT_s\right) + s\left(nT_s\right)\left(\sum_{k=1}^{\infty}\frac{\left(j2\pi f_c\right)^k\zeta_n^k}{k!}\right) = s\left(nT_s\right) + e\left(n\right) \quad (11)$$

and

$$e(n) = s\left(nT_s\right)\left(\sum_{k=1}^{\infty}\frac{\left(j2\pi f_c\right)^k\zeta_n^k}{k!}\right) \quad (12)$$

where $e(n)$ can be taken as an undesired quantity introduced only by the sampling jitter. $s(nT_s)$ is the desired signal component.

In this study, as shown in (11), we will take this additive model to simplify the problem and z_n can be rewritten as follows

$$z_n = s(nT_s) + e(n) \quad (13)$$

It is clear that, if we are able to estimate $e(n)$, from (13), $s\left(nT_s\right)$ can be reconstructed accordingly since z_n is available.

In the following, we will discuss the method to estimate the error term $e(n)$ from (12).

Examining (12), it is clear, if we know $s\left(nT_s\right)$ and the parameters f_c as well ζ_n, we can directly compute $e(n)$ from (12). Unluckily, $s\left(nT_s\right)$ is unknown. Assuming the estimation of the error term denoted as $\hat{e}(n)$, From (12) and (13), we have

$$\begin{aligned}\hat{e}\left(n\right) &= s\left(nT_s\right)\left(\sum_{k=1}^{\infty}\frac{\left(j2\pi f_c\right)^k\zeta_n^k}{k!}\right) \\ &= \left(z_n - \hat{e}(n)\right)\left(\sum_{k=1}^{\infty}\frac{\left(j2\pi f_c\right)^k\zeta_n^k}{k!}\right)\end{aligned} \quad (14)$$

Manipulating (14), we get

$$\begin{aligned}\hat{e}\left(n\right) &= \left(1+\sum_{k=1}^{\infty}\frac{\left(-j2\pi f_c\right)^k\zeta_n^k}{k!}\right)z_n\sum_{k=1}^{\infty}\frac{\left(j2\pi f_c\right)^k\zeta_n^k}{k!} \\ &= z_n\left[\sum_{k=1}^{\infty}\frac{\left(j2\pi f_c\right)^k\zeta_n^k}{k!} + \sum_{k=1}^{\infty}\frac{\left(-j2\pi f_c\right)^k\zeta_n^k}{k!}\sum_{k=1}^{\infty}\frac{\left(j2\pi f_c\right)^k\zeta_n^k}{k!}\right]\end{aligned} \quad (15)$$

From (15), since z_n, f_c as well ζ_n are known, the error term can be determined accordingly.

As the result, the sampled signal can be reconstructed as follows

$$\hat{s}\left(nT_s\right) = z_n - \hat{e}\left(n\right) \quad (16)$$

In the following, we will study the effective implementation of (16). It is observed that, from (15), the estimation of error term can be implemented in a cascade structure and online manner. The specific derivation is illustrated as follows.

Let's define

$$a = j2\pi f_c \quad (17)$$

Then,(15) can be rewritten as

$$\hat{e}(n) = z_n\left[\sum_{k=1}^{\infty}\frac{a^k\zeta_n^k}{k!} + \sum_{k=1}^{\infty}\frac{\left(-a\right)^k\zeta_n^k}{k!}\sum_{k=1}^{\infty}\frac{a^k\zeta_n^k}{k!}\right] \quad (18)$$

It is noted that the higher order errors terms in (18) contribute less to the total error $\hat{e}(n)$ comparing the less order errors terms, to simple the error analysis, we approximate error term $\hat{e}(n)$ using the first n+1 order terms and neglect higher error terms when operate n order Taylor expansion in

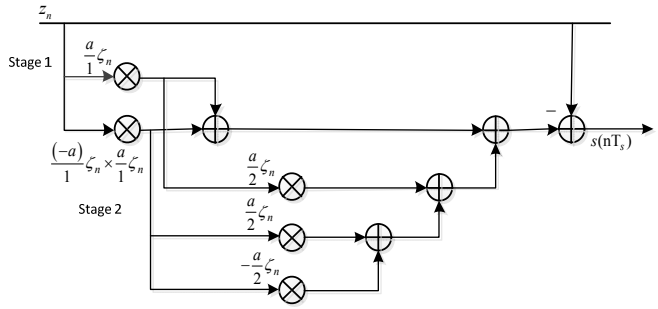

Figure 2. The proposed multistage cascade multiplier model (two stages)

(18).

Then, we get n^{th} order Taylor expansion of (18) as

$$\hat{e}(n) \approx z_n \begin{bmatrix} \sum_{k=1}^{n} \frac{a^k}{k!}\zeta_n^k + \frac{(-a)}{1!}\zeta_n^1 \sum_{k=1}^{n} \frac{a^k}{k!}\zeta_n^k \\ + \frac{(-a)^2}{2!}\zeta_n^2 \sum_{k=1}^{n-1} \frac{a^k}{k!}\zeta_n^k \\ \vdots \\ + \frac{(-a)^n}{n!}\zeta_n^n \sum_{k=1}^{1} \frac{a^k}{k!}\zeta_n^k \end{bmatrix} \quad (19)$$

where n in $\hat{e}(n)$ denotes reconstructed error term using n^{th} order Taylor expansion. Similarly, $(n\text{-}1)^{th}$ order Taylor expansion of (18) can be denoted as

$$\hat{e}(n-1) \approx z_n \begin{bmatrix} \sum_{k=1}^{n-1} \frac{a^k}{k!}\zeta_n^k + \frac{(-a)}{1!}\zeta_n^1 \sum_{k=1}^{n-1} \frac{a^k}{k!}\zeta_n^k \\ + \frac{(-a)^2}{2!}\zeta_n^2 \sum_{k=1}^{n-2} \frac{a^k}{k!}\zeta_n^k \\ \vdots \\ + \frac{(-a)^{n-1}}{(n-1)!}\zeta_n^{n-1} \sum_{k=1}^{1} \frac{a^k}{k!}\zeta_n^k \end{bmatrix} \quad (20)$$

Then, let's define the error difference $\hat{e}_n(n)$, substituting (19) and (20), we get

$$\hat{e}_n(n) = \hat{e}(n) - \hat{e}(n-1)$$

$$= z_n \begin{bmatrix} \frac{a^n}{n!}\zeta_n^n + \frac{(-a)^1}{1!}\zeta_n^1 \left(\frac{a^n}{n!}\zeta_n^n\right) \\ + \frac{(-a)^2}{2!}\zeta_n^2 \left(\frac{a^{n-1}}{(n-1)!}\zeta_n^{n-1}\right) \\ \vdots \\ \frac{(-a)^n}{n!}\zeta_n^n \left(\frac{a}{1}\zeta_n\right) \end{bmatrix} \quad (21)$$

To further simplify the notations, we define

$$e_{n0}(n) = z_n \times \frac{a^n}{n!}\zeta_n^n$$

$$e_{n1}(n) = z_n \left(\frac{(-a)^1}{1!}\zeta_n^1\right)\left(\frac{a^n}{n!}\zeta_n^n\right)$$

$$e_{n2}(n) = z_n \left(\frac{(-a)^2}{2!}\zeta_n^2\right)\left(\frac{a^{n-1}}{(n-1)!}\zeta_n^{n-1}\right) \quad (22)$$

$$\vdots$$

$$e_{nn}(n) = z_n \left(\frac{(-a)^n}{n!}\zeta_n^n\right)\left(\frac{a}{1}\zeta_n\right)$$

With the definitions in (22), we can obtain the following

$$e_{n0}(n) = e_{(n-1)0}(n-1) \times \frac{a}{n}\zeta_n$$

$$e_{n1}(n) = e_{(n-1)1}(n-1) \times \frac{a}{n}\zeta_n$$

$$e_{n2}(n) = e_{(n-1)2}(n-1) \times \frac{a}{n-1}\zeta_n \quad (23)$$

$$\vdots$$

$$e_{n(n-1)}(n) = e_{(n-1)(n-1)}(n-1) \times \frac{a}{2}\zeta_n$$

$$e_{nn}(n) = e_{(n-1)(n-1)}(n-1) \times \left(-\frac{a}{n}\right)\zeta_n$$

As the result, with (23), (21) can be rewritten as

$$\hat{e}_n(n) = e_{n0}(n) + e_{n1}(n) + e_{n2}(n) + \ldots + e_{nk}(n) + \ldots + e_{nn}(n) \quad (24)$$

It is noted that the *n*order error term $\hat{e}(n)$ can be calculated by $(n\text{-}1)^{th}$ order term $\hat{e}(n-1)$ and error difference $\hat{e}_n(n)$ using (21),(23), and (24).

For illustrating purpose, we take 2^{nd} order Taylor expansion as an example.

When n=2, from (21),we get

$$\hat{e}(2) = \hat{e}_2(2) + e(1) \quad (25)$$

where $e(1)$ can be calculated as follows using (19),

$$e(1) = z_n \left[\frac{a}{1}\zeta_n + \frac{(-a)}{1}\zeta_n \times \frac{a}{1}\zeta_n\right] \quad (26)$$

From the definition in (23), we have

$$e_{10}(1) = z_n \times \frac{a}{1}\zeta_n, e_{11}(1) = z_n \times \frac{(-a)}{1}\zeta_n \times \frac{a}{1}\zeta_n \quad (27)$$

From (24), we have

$$e_2(2) = e_{20}(2) + e_{21}(2) + e_{22}(2) \quad (28)$$

From (23), we can calculate the followings

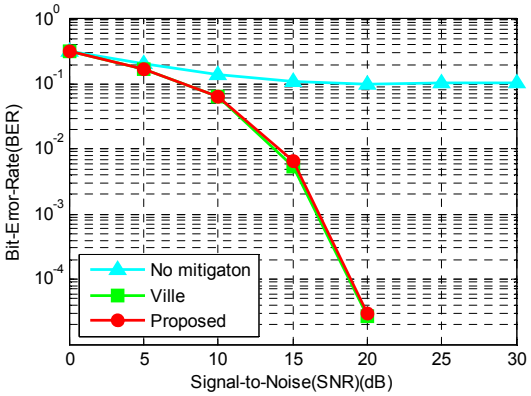

Figure 3. BER performance of the fixed RMS jitter of 20ps

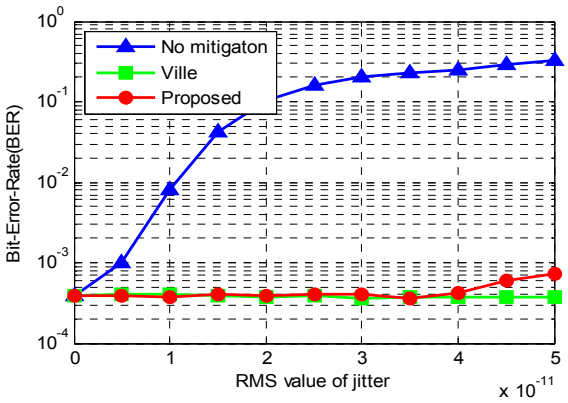

Figure 4. BER performance of the fixed SNR of 18dB with two stages reconstruction system

$$e_{20}(2) = e_{10}(1) \times \frac{a}{2}\zeta_n$$
$$e_{21}(2) = e_{11}(1) \times \frac{a}{2}\zeta_n \qquad (29)$$
$$e_{22}(2) = e_{11}(1) \times \left(-\frac{a}{2}\right)\zeta_n$$

Substituting (29) into(28) and (25), we get

$$\hat{s}(nT_s) = z_n - \hat{e}(2) \qquad (30)$$

The implementation of (30) is shown in Figure 2. In this compensation system, we use only multiplier whose coefficients contain the jitter estimation value obtained .The idea of the cascade is based on the fact that the compensation system can be further improved by adding the Taylor expansion terms for the reconstruction quality needed. The proposed method named as CM-SJM method .As discussed above, the implementation costs of the proposed sampling jitter mitigation system are reduced since only multipliers need to be adapted when carrier frequency f_c and the sampling jitter ζ_n observed changes over time. On the other hand, the precision of sampling mitigation could be improved by adding the stages of cascade.

VI.SIMULATION RESULTS

The following simulation results are performed in LTE uplink system with 10MHz bandwidth[9]. At first, the input data stream is constellated to single carriers symbols by using 16-QAM.Then the symbols converted into parallel symbols and preceded by DFT. Then, the symbols become the input of the blocks of SC-FDMA. here we use 1024 subcarriers, including 600 subcarriers are active, 15kHz subcarrier spacing and normal cp(cyclic prefix) is added. After the baseband signal has been produced, we use 2.6GHz carriers to transmit the SC-FDMA signal, and the signal is filtered by plain additive white Gaussian noise (AWGN). At the receiving end, we use an bandpass filter to filter the noise out of band.

Then we use sub-sampling frequency of 16*1024*15kHz = 245.76 MHz. After the sampling, the proposed jitter cancellation method is applied. Then the SC-FDMA

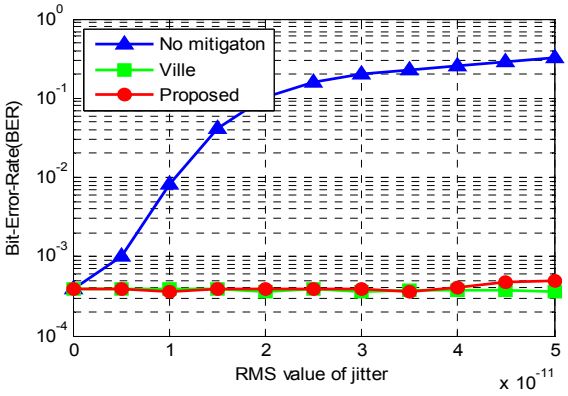

Figure 5. BER performance of the fixed SNR of 18dB with three stages reconstruction system

waveform is detected and the bit- error-rates are evaluated as performance indicators.

The performance comparison method is proposed in[7].

Experiment 1: This experiment is carried out to evaluate the BER performance of the proposed CM-SJM method. In this experiment, we use two stages cascade structure (*n*=2). Figure 3 shows the BER performance versus SNR. From the results illustrated by the line with triangle, we can observe that the sampling jitter have an adverse effect on receiver system under different SNR conditions. Even in high SNR level, BER of the system without sampling jitter mitigation is also quite high. Moreover, under this simulation conditions, our proposed CM-SJM method gives a very close performance with reference method[7], which greatly mitigates the adverse effect of the sampling jitter.

Experiment 2: This experiment is carried out to evaluate the BER performance in different jitters RMS for our proposed CM-SJM method using two stages structure (*n*=2). The SNR is fixed to 18dB. The simulation results are illustrated in Figure 4. We can conclude from Figure 4 that our proposed CM-SJM method give a quite good compensation performance when the RMS value of jitter below 40ps, but its performance is inferior to that of the compared method when the sampling jitter is larger than 40ps.

Experiment 3: This experiment is carried out to evaluate the BER performance of the proposed CM-SJM method in different jitters RMS with three stages structure (n=3). The simulation results are illustrated in Figure 5. It is clear to see that the BER with three stages structure is better than that of the two stage structure shown in Figure 4. This means the performance of the proposed CM-SJM method can be improved by adding more cascade stages but with increasing the implementation cost. Specifically, from Figure 5, it is encouraged to see that even in 50ps, our proposed CM-SJM method is able to give good performance, only a slightly decline after the sampling jitter is above 40ps. Compared to the Ville method in [7], our proposed method is much more efficient and flexible in implementation.

From this observation, we can conclude that our proposed CM-SJM method with three stages structure is able to provide required sampling jitter compensation performance even in demanding environment.

VII. CONCLUSIONS

Sampling jitter is an important problem for direct RF sampling receivers. Simulation shows that sampling jitter has huge effect on the performance of direct RF sampling receivers. This paper proposed a novel method to mitigate the effect of it. The main advantage of our proposed method is that the compensation system using only multipliers, which greatly reduce the implementation cost and complexity. On the other hand, since the derivation of our propose method is based on the general form of input signal, which means our proposed jitter mitigation method have no demand on special signal type, which can meet the demand of multi-standard communications. Simulation results show that our proposed CM-SJM method with three stages structure is able to provide required sampling jitter compensation performance

even in demanding environment.

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