# FPGA Implementation of Digital Up/Down Convertor for WCDMA System

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***Abstract*— In this paper, we present FPGA implementation of a digital down convertor (DDC) and digital up convertor (DUC) for a single carrier WCDMA system. The DDC and DUC is complex in nature. The implementation of DDC is simple because it does not require mixers or filters. Xilinx System Generator and Xilinx ISE are used to develop the hardware circuit for the FPGA. Both the circuits are verified on the Virtex-4 FPGA.**

***Keywords*— WCDMA, FPGA, DDS, FIR**

## I. INTRODUCTION

Digital down convertor (DDC) and Digital up convertor (DUC) are extensively used in the radio systems. They are more popular than their analogue counterparts because of small size, low power consumption and accurate performance. The DDC converts the signal at the output of analog to digital convertor (ADC), centered at the intermediate frequency (IF), to complex baseband signal. In addition, DDC also decimates the baseband signal without affecting its spectral characteristics. The decimated signal, with a lower data rate, is easier to process on a low speed DSP processor. Similarly, the DUC converts a baseband signal to a passband IF signal. The functional behaviors of the two circuits are therefore equal and opposite.

This paper discusses the DDC and DUC for the WCDMA system and implements them on the field programmable gate array (FPGA). WCDMA is a leading choice of data communication in the wireless industry nowadays and is selected as the air interface for the UMTS. WCDMA supports a higher data rate then CDMA and is less susceptible to narrowband interferers and multipath fading. Similarly, FPGAs are used for real time implementation of the signal processing algorithms, particularly related to communication, because of their high speed and accurate performance.

We have organized this paper as follows. Section II presents the working principle and FPGA design of the DUC. In section III, we discuss the FPGA implementation of the DDC. Experimental results are given in Section IV. Finally, this paper is concluded in Section V.

## II. DIGITAL UP CONVERTOR

Digital up converter (DUC) converts a baseband low data rate signal to a high data rate intermediate frequency (IF) signal. This is done by first up-sampling the baseband signal to the required sampling frequency and then mixing it with the high frequency carrier. A functional diagram of the DUC is given in Figure 1.

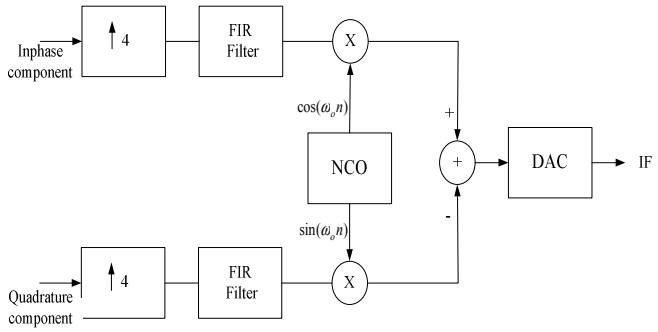


**Figure 1. Block diagram of digital up convertor**

The DUC has two identical data paths, one for the inphase and the other for quadrature input. For this reason, it is also referred to as a complex DUC. The baseband signal at 23.04 Msps is upsampled by 4 to 98.16 Msps before mixing with the numerically controlled oscillator (NCO) output, to produce the spectrum centered around the desired modulation frequency. The lowpass FIR filter acts as an anti-alaising filter after upsampling. The specifications of this FIR filter are given in Table 1.

**Table 1. Specifications for FIR filter in DUC**

| | |
|---|---|
| Stopband frequency | 20 MHz |
| Passband frequency | 5 MHz |
| Passband ripple | 0.1 dB |
| Stopband ripple | 140 dB |

Figure 2 shows the circuit for the DUC realized on FPGA. MATLAB FDATool together with the Xilinx FIR Compiler is used to create a lowpass filter having the above frequency response. The Xilinx DDS Compiler generates the IF carrier frequency signal. Direct digital synthesizer (DDS), a digital version of the NCO, provides an accurate programmable frequency up to 450 MHz.

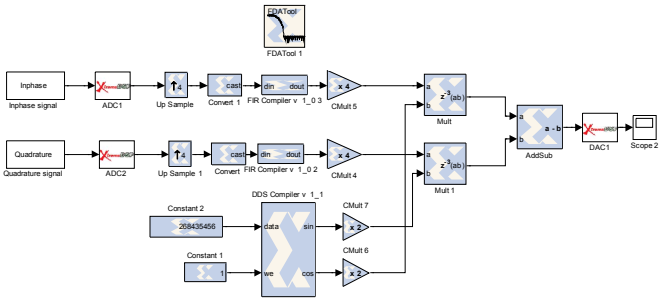


**Figure 2. System Generator implementation of the digital up convertor**

## III. DIGITAL DOWN CONVERTOR

The DDC performs the reverse function of the DUC. It converts an IF signal to the baseband signal. The DDC is built in a similar manner as DUC, but it uses down-sampling instead of up-sampling and they are connected in the reverse order compared to the DUC. This paper uses the DDC as described in [1] for the FPGA implementation. A functional block diagram of the DDC is shown in Figure 3. This DDC does not require mixers or low pass filters [1].

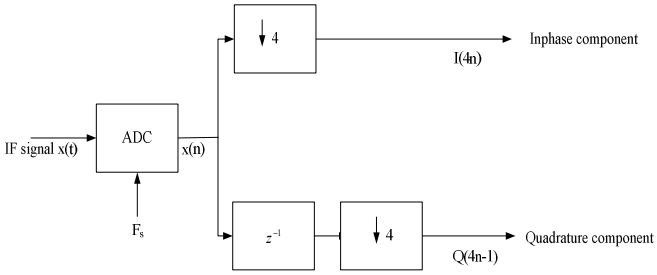


**Figure 3. Block diagram of digital down convertor**

The IF signal $x(t)$ is sampled at 98.16 Msps by the ADC to create a digitized IF signal $x(n)$. This signal is de-multiplexed into two data streams. One signal stream is downsampled by 4 to produce an inphase signal $I(4n)$, while the other stream, delayed by a single sample, gives the quadrature component $Q(4n-1)$ on downsampling. The data rate of resultant inphase and quadrature signals is 23.04 Msps. Mathematical analysis of DDC is given in the Appendix. Figure 4 shows the circuit diagram of the DDC. An additional inverting amplifier is applied to both the signal streams to counter a delay of $\pi$ radians introduced by the ADC on FPGA.

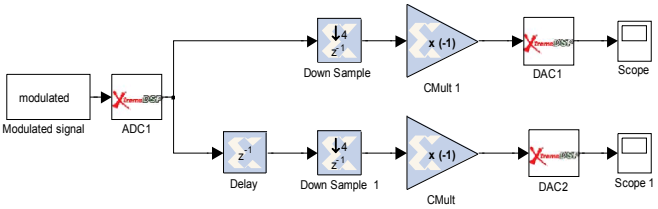


**Figure 4. System Generator implementation of the digital down convertor**

## IV. EXPERIMENTAL RESULTS

The DDC and DUC circuits created using the Xilinx System Generator are finally converted to bit file using the Xilinx ISE. This bit file is programmed on the XtremeDSP development kit-IV using the Xilinx ChipScope programming and debugging tool. The FPGA used is Virtex-4 (XC4VSX35-10FF668). Figure 5 shows the block diagram of the laboratory test bench. WCDMA signal at IF 23.04 MHz is generated using the signal generator and applied to the ADC. The spectrums of the desired signals are displayed using the spectrum analyzer. The parameters used in the test bench are listed in Table 2.

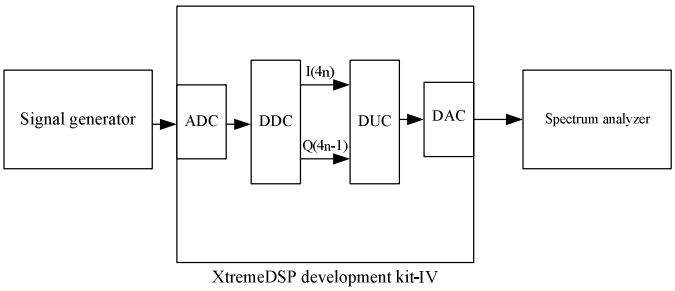


**Figure 5. Laboratory test bench**

**Table 2. Parameters used in test bench**

| Parameter | Value |
|---|---|
| FPGA | Xilinx Virtex-4 (XC4VSX35-10FF668) |
| FPGA clock frequency | 92.16 MHz |
| ADC sampling frequency | 92.16 MHz |
| DAC sampling frequency | 92.16 MHz |
| Input data rate | 3.84 Msps |
| IF frequency | 23.04 MHz |

Figure 6 shows the spectrum of the baseband signal at the output of DDC. The bandwidth of this signal is 2.5 MHz. Similarly, Figure 7 gives the spectrum of the IF signal at the output of DUC. A brief summary of FPGA resource utilization as given by Device Utilization Summary in Xilinx ISE is given in Table 3.

**Table 3. FPGA resource utilization**

| Logic utilization | Used | Available | Utilization |
|---|---|---|---|
| Number of Slice FlipFlops | 3,373 | 30,720 | 10% |
| Number of 4 input LUTs | 3,575 | 30,720 | 11% |
| Number of DSP48s | 60 | 192 | 31% |

An important parameter in the resource utilization summary is the consumption of the DSP48 blocks. The DSP48 blocks are highly efficient blocks created specifically for the DSP applications and use the Xilinx Virtex-4 devices.

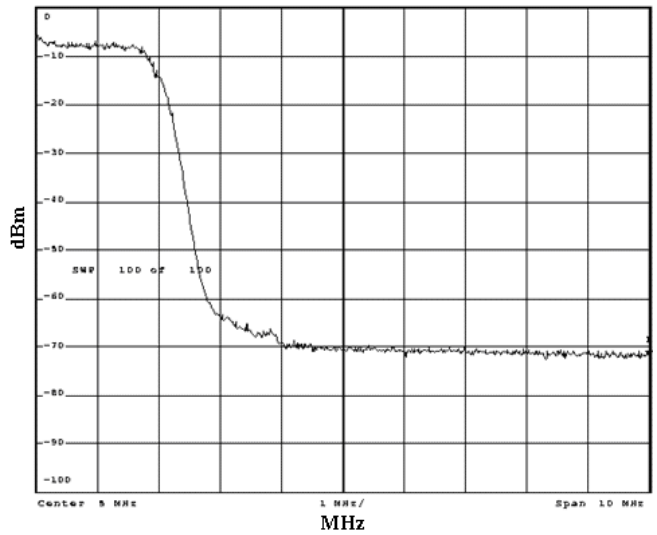


**Figure 6. Spectrum of demodulated WCDMA signal**

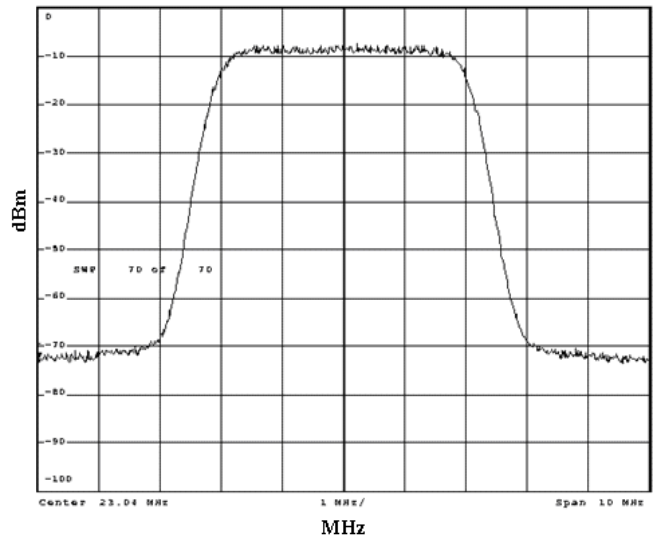


**Figure 7. Spectrum of modulated WCDMA signal**

## V. CONCLUSION

In this paper we have presented an implementation of the DDC and DUC on the Virtex-4 FPGA. FPGA is found suitable for the real time implementation of the communication algorithms because of their high performance, small size, flexibility and competitive price. The DDC and DUC circuits are implemented using the Xilinx System Generator design tool. Experimental results verify the working of the designed circuits.

## APPENDIX

$$x(n) = I(n)\cos\left(\frac{\pi}{2}n\right) - Q(n)\sin\left(\frac{\pi}{2}n\right) \tag{1}$$

$$\begin{aligned} x(n-1) &= I(n-1)\cos\left(\frac{\pi}{2}(n-1)\right) - Q(n-1)\ \sin\left(\frac{\pi}{2}(n-1)\right) \\ &= I(n-1)\sin\left(\frac{\pi}{2}n\right) + Q(n-1)\cos\left(\frac{\pi}{2}n\right) \end{aligned} \tag{2}$$

**Inphase component**

$$\begin{aligned} x(n-2) &= I(n-2)\ \sin\left(\frac{\pi}{2}(n-1)\right) - Q(n-2)\cos\left(\frac{\pi}{2}(n-1)\right) \\ &= -I(n-2)\cos\left(\frac{\pi}{2}n\right) + Q(n-2)\sin\left(\frac{\pi}{2}n\right) \end{aligned}$$

Downsampling by a factor of 4,

$$\begin{aligned} x(4n-2) &= -I(4n-2)\cos\left(\frac{4\pi}{2}n\right) + 0 \\ &= -I(4n-2) \end{aligned}$$

Passing through the inverter, we get the inphase component

$$x(4n-2) = I(4n-2)$$

**Quadrature component**

From Equation (2),

$$\begin{aligned} x(n-2) &= I(n-2)\ \sin\left(\frac{\pi}{2}(n-1)\right) - Q(n-2)\ \cos\left(\frac{\pi}{2}(n-1)\right) \\ &= -I(n-2)\cos\left(\frac{\pi}{2}n\right) + Q(n-2)\sin\left(\frac{\pi}{2}n\right) \end{aligned} \tag{3}$$

Delaying Equation 3 by one sample,

$$x(n-3) = -I(n-3)\sin\left(\frac{\pi}{2}n\right) - Q(n-3)\cos\left(\frac{\pi}{2}n\right)$$

Downsampling by a factor of 4,

$$x(4n-3) = -Q(4n-3)$$

Passing through an inverter,

$$x(4n-3) = Q(4n-3)$$

## REFERENCES


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