Effect of Higher-order PSDs on Timing Jitter

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Abstract: The effect of higher-order power spectral densities (PSDs) at the squarer output on timing jitter is described in this paper. A timing circuit is placed at the receiving filter output and consists of a squarer, a pre-filter, a phase-locked loop (PLL) and a zero cross detector (ZCD) arranged in tandem. The pre-filter and the PLL are collectively referred to as the extractor. The ZCD generates pulse waveforms at the zero crossings of the sinusoidal wave at the PLL output. The phase of the sinusoidal wave fluctuates due to the randomness of the signal and the presence of noise. This fluctuation is referred to as timing jitter. The transmission schemes are assumed to be pulse-amplitude modulation, amplitude-shift keying and quadrature amplitude modulation. Additive Gaussian white noise exists at the receive filter input. The band-limiting scheme is assumed to be a cosine roll-off. The higher-order PSDs are components of the jitter source PSD at the squarer output. The jitter source PSD consists of SS, SN, and NN components. The SS component arises from the cross product of the signal with itself and is often referred to as self-noise or pattern noise. The SN component arises from the cross product of the signal and the noise, and the NN component arises from the cross product of the noise with itself. Both the SS and SN components of the jitter source PSD can be represented as a sum of PSDs with different orders since the signal passing through the timing circuit is in a broad sense a cyclostationary process. By its nature, the NN component does not have any higher-order PSDs since it originates from the addition of white Gaussian noise, which can be thought of as a stationary process. The jitter PSD at the PLL output also has SS, SN, and NN components since it can be represented by a linear combination of the jitter source PSD at the squarer output and the extractor transfer function. Each component of the jitter variance can be obtained by integrating the corresponding component of the jitter PSD over a finite range.

The authors discuss the effect of higher-order PSDs on the jitter variance at the PLL output in order to obtain a clear understanding of the jitter performance. Theoretical calculations show that the SS and SN components of the jitter source PSD can be represented by 0th and ±2nd order PSDs. However, based on numerical calculations, the SN component consists of only the 0th order PSD and thus can be regarded as a stationary process. This may be due to the effect of the band-limiting scheme.

The results hold for all of the transmission schemes, SNRs, alphabet sizes, and roll-off factors treated in this paper and thus these are expected to be useful for evaluating the jitter performance and the jitter generation mechanism.