Design of Small-Area Transimpedance Optical Receiver Module for Optical Interconnects

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***Abstract*—The development and miniaturization of electronic devices and components is pushing the system devices and their interconnecting interfaces to become even smaller. Thus, reducing the size of receiver (Rx) and transmitter (Tx) chips plays an plays an important role in designing a small-size optical modules utilized in o/e and e/o converters. Therefore, designing a small-area optical Rx may require intuitive solutions, such as building single-ended Rx and utilizing some of the advantages of differential Rx. Optical Rx should convert optical input signal to voltage output signal and provide sufficient gain and frequency operation for feeding to subsequent blocks including clock and data recovery circuit (CDR) and/or Serializer and Deserializer (SerDes). Therefore, we have designed a small-area transimpedance optical receiver (TIORx) using regulated-cascode (RGC) as an input stage which converts input photocurrent to voltage signal. The RGC block is connected to post amplifying stages to increase the overall transimpedance gain of the TIORx. The post amplifying gain stages utilizes two intersecting active feedback in order to increase the frequency operation in addition to increasing the gain of the proposed TIORx chip. The TIORx module is designed in a 0.13µm CMOS technology and works up to 10 Gbps data rate. The TIORx chip core occupies an area of 0.051mm^2 with power consumption of 16.9 mW at 1.3 V. A measured 3-dB bandwidth of 6.9 GHz was obtained for the TIORx module with a transimpedance gain of 60 dBΩ.**

***Keyword*—Optical receiver, small-area circuit design, bandwidth improvement, optical interconnections**

I. INTRODUCTION

As the data rate of internet traffic is increasing the electrical interconnection cannot provide reliable data at higher frequencies due to its limitations at high frequency operation [1]. Thus, optical interconnection is dominating the market because of its advantages such as low electromagnetic interference (EMI), negligible insertion loss with inner-channel crosstalk for multi-channel optical link and light weight comparing to electrical interconnection at high data rates. Hence, optical interconnection system is being widely utilized in high data rate video and data transmission systems [2]. However, optical interconnection also requires electrical-to-optical (e/o) and optical-to-electrical (o/e) converters. Designing a small-size o/e and e/o converters is important. Thus, reducing the size of receiver (Rx) and transmitter (Tx) chips plays an plays an important role in designing a small-size optical modules utilized in o/e and e/o converters. Since, the development and miniaturization of CMOS technology is pushing the design limits to design even smaller electronic devices and their interconnecting interfaces. Thereby, requiring the reduction of optical modules of o/e and e/or converters utilized in applications such as small form-factor pluggable (SFP) and system in package (SiP) systems for board-to-bard, chip-to-chip and rack-to-rack optical interconnection [3-4].

Designing of a compact optical Rx circuits for high-speed operation is important to reduce the signal propagation loss and reduce the active are used for chip design. Hence, designing of small-area optical Rx modules may require intuitive solutions, such as utilizing some of the advantages of differential Rx in designing of a single-ended Rx modules. Optical Rx chip should also be able to provide a sufficient gain and frequency operation with reduced size for feeding the signal to post-processing blocks such as CDR and/or SerDes [5]. In our previous work, we have analyzed the performance of single-ended and differential Rx in terms noise, power, size, and gain [6]. From comparison of single-ended and differential topology in table 1, the single-ended Rx chip size showed much smaller size. Hence, the size of Rx module can be significantly reduced by using a single-ended Rx. However, the data rate of single-ended Rx module was relatively small comparing differential topology. Therefore, we have tried to improve the performance single-ended Rx by increasing the data rate of Rx using he Rx chip [7].

In an optical Rx design, the transimpedance amplifier (TIA) plays the role of a front-end amplifier for amplifying the weak

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current signals generated from the photodiode (PD) and converting to voltage signal which would be fed to subsequent blocks (limiting amplifier or clock and data recovery circuit). The conventional Rx module consists of a TIA preamplifier block, limiting amplifier, and an output buffer. TIA design using inductive peaking for bandwidth enhancement and high data rate operation has been proposed in [8]. However, the excessive size of the inductor makes the total chip size big. An inductorless TIA has been designed in [9], where several shunt feedback TIAs connected in parallel were suggested for bandwidth improvement and chip size reduction. However, this design method has high power consumption due to the several TIAs deployed. In conventional Rx circuits, the TIA may not have enough gain and bandwidth to drive other circuits and as a result, may require the use of LA, equalizer [10-11], and other performance enhancement circuitry. However, due to the need for high data-rate and high performance operation, the need for the additional circuitry (LA, equalizer, etc.) will result to the increase in circuit complexity and thus, lead to increase in total chip area and increase in overall power consumption.

In this work, we propose a small area, high data-rate and inductorless TIORx which combines some of the advantages of both the TIA and Rx. While acting as a front-end amplifier for the weak signals from the PD, it also incorporates the gain and bandwidth enhancement advantages of an LA, in a conventional Rx. Thus, due to the absence of a dedicated LA stage, the TIORx module reduces the total chip area, while improving the gain and bandwidth performance. In our proposed design, the TIORx is made up of a regulated cascode (RGC) input stage; an inter-stage buffer; a gain stage with intercepting active feedbacks; and an output stage (which acts as a buffer). The RGC input stage has been utilized to reduce the input capacitance effect from the PD while improving the bandwidth [12]. The inter-stage buffer used between RGC and gain stage reduces parasitic capacitance at the output of RGC block, thereby improving bandwidth performance. The post amplifying stages utilizes active feedback only, making the chip less sensitive to process changes compared to a passive feedback system. The fabricated TIORx achieves a transimpedance gain of 60 dBΩ and occupies an area of 50.6 μm^2, which is quite small when compared to other high data-rate optical receivers of similar CMOS technology.

II. The TIORx Circuit Design

The TIORx is designed in a 0.13μm CMOS technology and the schematic of the TIORx chip is shown in Fig. 1. The input stage, which is the RGC, consists of transistors M_1 and M_2.The RGC input stage reduces the input impedance by the amount of its own voltage gain, which prevents the input pole from dominating the TIORx bandwidth and reduces capacitive effect of the PD [5]. Thus, the RGC circuit can be used effectively for CMOS integration as a front-end amplifier. The input impedance of RGC stage is given as [12]:

$$Z_{IN-RGC} = \frac{1}{gm_2(1+gm_1R_1)}, \quad (1)$$

where $1+gm_1R_1$ is the gain of the local feedback and with the product of the common gate stage, it behaves as a large transconductor $G_m=gm_2(1+gm_1R_1)$. Thus, the size of local feedback decides the amount of reduction of input parasitic capacitance effect for bandwidth determination. The RGC peaking frequency in frequency response is given as:

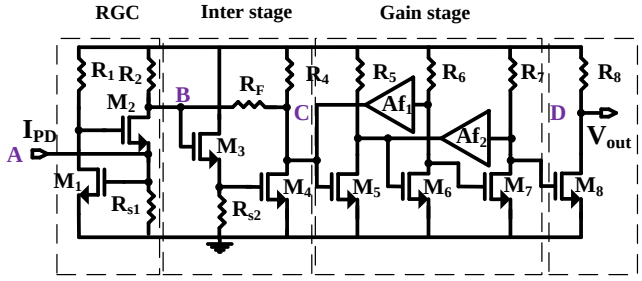


Fig. 1. (a) Schematic of TIORx.

$$f_{peak} = \frac{1}{2\pi R_1(C_{gs2}+C_{gd1})}. \quad (2)$$

At low frequency, the open-loop transimpedance gain of the TIORx is given as:

$$Z_{IN-GAIN} = -(R_2 \| R_F)\frac{gm_3R_{s2}}{(1+gm_3R_{s2})}\left(gm_4 \| gmf_1\right) \quad (3)$$
$$R_4\left(gm_5 \| gmf_2\right)R_5gm_6R_6gm_7R_7gm_8R_8$$

The TIORx is made up of four stages, namely, an input stage (which consists of the RGC); an inter-stage; a gain stage with intercepting active feedbacks; and an output stage (which acts as the buffer). The RGC block is important in the TIORx circuit as it affects the input noise and the stability of the whole TIORx circuit while delivering the input photo current to the output with increased gain. Thus, the design parameters have to be carefully chosen not to interfere with the input impedance for high frequency operation.

M_3 and M_4 make up the inter-stage stage of the TIORx, where high frequency operation should be maintained for delivering the converted input current to output voltage for the gain stage. The impedance at the drain of M_2 (of RGC stage) and M_4 (of inter-stage) are reduced by factor of *1+A* by R_F shunt feedback and correspondingly, the poles are sped up by the factor, *1+A*. A common-drain (CD) is placed at the drain of M_2 because the capacitive effect on bandwidth is small [12]. The inter-stage isolates the RGC input stage from the gain stage and also adjusts the input dc level from the RGC stage.

To increase the overall gain of the TIORx to higher output voltage levels, several common source (CS) amplifying stages (M_5 – M_7) have been utilized. However, placing these CS gain stages may reduce the bandwidth. Thus, to increase the bandwidth while maintaining a high gain level, two intersecting active feedback stages have been utilized [13]. The negative

active feedback utilized in the gain stage is different from the conventional resistive feedback which avoids the direct resistive load to the preceding transimpedance stage. Moreover, active devices suffer less process variations than passive devices during fabrication. Hence, adding the active feedback stages, Af_1 and Af_2, compensate by peaking at high frequencies. The high-frequency peaking occurs at Af_1 and Af_2 active feedback. The peaking of the first and second active feedbacks is given as:

$$f_{peak,f1} = \frac{1}{2\pi R_4 (C_{gd6} + C_{gdf1})} \tag{4}$$

$$f_{peak,f2} = \frac{1}{2\pi R_5 (C_{gd7} + C_{gdf2})} \tag{5}$$

As the circuit is more complex, we separate the circuit from point A to B, B to C and C to D as shown in Figure 1. Firstly, the poit from I_{in} to I_B is the core RGC block, front-end of TIA circuit, which has an important effect in the input noise and stability of the whole Rx circuit and delivers the input photo current to the output with increased gain. Thus, the design parameters have to be carefully chosen to interfere with the input impedance for high frequency operation. The transfer function can be derived as follows:

$$\frac{I_B}{I_{in}}(s) = \frac{1+\frac{sC_1}{gm_1}}{\left[1+\frac{s(C_{gs1}+C_{sb1})}{(1+gm_1R_1)gm_2}\right]\left[1+sR_1\left(C_1+C_{gs2}+C_{gd2}\right)\right]} \tag{6}$$

The next point is from I_B to V_C is inter-stage block, where the high frequency operation should be maintained for delivering the converted input current to output voltage for the gain stage. The impedance of drain M_2 and M_4 are reduced by factor of (1+A) by R_F shunt feedback and correspondingly the poles has been speed up by the factor (1+A). The common-drain (CD) is placed at the drain of M_2 because the capacitive effect on bandwidth is small [12]. The transfer function from B to C is with simplification of R_1 and R_f parallel resistors, is given as follows:

$$R_F^{'} = (R_1 \,||\, R_F)\frac{1}{1+\left(\frac{gm_3R_{s2}}{1+gm_3R_{s2}}\right)gm_4R_4}$$

$$\frac{V_C}{I_B}(s) = \frac{gm_3gm_4R_{s2}R_4R_F^{'}}{1+gm_3R_{s2}}\left(1+\frac{sCgs3}{gm3}\right) \tag{7}$$

$$\frac{1}{\left[1+\frac{s(R_F^{'}C_{gs3}+gm_3R_{s2}R_F^{'}C_1^{*}}{1+gm_3R_{s2}}\right]}\frac{1}{\left[1+\frac{s\left(C_{gs3}+C_{gs4}\right)}{gm_3}\right]}$$

The intersecting active feedback from V_C to V_{out} is the gain stage, where the voltage input has been increased to higher output voltage levels. Adding the negative active feedback increases the 3-dB bandwidth. The active feedback effects of Af_1 and Af_2 has been included in the transfer function and the equation is given as:

$$\frac{V_{out}}{V_C} = \frac{G_5(s)G_6(s)G_7(s)}{1+G_5(s)G_6(s)Gf_1(s)+G_6(s)G_7(s)Gf_2(s)} = \frac{G^3(s)}{1+2G^2(s)Gf(s)} \tag{8}$$

with the assumption $G_5(s) = G_6(s) = G_7(s) = \frac{GmR}{1+sRC}$, and $Gf_1(s) = Gf_2(s) = Gf(s) = \frac{GmfR}{1+sRC}$.

The last stage capacitance effect is loaded by input capacitance of output buffer. After combining the equations (6) to (8) we can write the transfer function of Rx as:

$$\frac{V_{out}}{I_{in}} = \frac{I_B}{I_{in}} * \frac{V_C}{I_B} * \frac{V_{out}}{V_C} =$$

$$\frac{1+\frac{sC_1}{gm_1}}{\left[1+\frac{s(C_{gs1}+C_{sb1})}{(1+gm_1R_1)gm_2}\right]\left[1+sR_1\left(C_1+C_{gs2}+C_{gd2}\right)\right]} \tag{9}$$

$$\frac{gm_3gm_4R_{s2}R_4R_F^{'}}{1+gm_3R_{s2}}\left(1+\frac{sCgs3}{gm3}\right)\frac{1}{\left[1+\frac{s(R_F^{'}C_{gs3}+gm_3R_{s2}R_F^{'}C_1^{*}}{1+gm_3R_{s2}}\right]}$$

$$\frac{1}{\left[1+\frac{s\left(C_{gs3}+C_{gs4}\right)}{gm_3}\right]}\frac{G^3(s)}{1+2G^2(s)Gf(s)}$$

The transimpedance gain of the TIORx can be obtained from equation (9) and is written as follows:

$$Z_T(0) = \frac{gm_3gm_4R_{s2}R_4}{1+gm_3R_{s2}} * \left[R_1 \,||\, \frac{R_F}{1+\left(\frac{gm_3R_{s2}}{1+gm_3R_{s2}}\right)gm_4R_4}\right] \tag{10}$$

The 3-dB bandwidth of the TIORx is affected by dominant poles at amplifying stages of gm_3, gm_5 and gm_6. Thus, the dominant poles can be described by the frequency response of the gain stages with transconductance of the dominant poles given by the time constant equations of (11) to (15):

$$\tau_{eq} = \tau_3 + \tau_5 + \tau_6 \tag{11}$$

$$\tau_3 = \left(R_F \,||\, \frac{1}{gm_3}\right)\underbrace{\left[C_{s3}+C_{gs4}+\left(1+gm_4R_4\right)C_{gd4}\right]}_{\alpha_1} = \left(R_F \,||\, \frac{1}{gm_3}\right)\alpha_1 \tag{12}$$

$$\tau_5 = \left(\left(R_4 + \frac{1}{gm_4}\right) \| \frac{1}{gmf_1}\right) \underbrace{\left[C_{s5} + C_{gs6} + (1 + gm_6 R_6) C_{gd6}\right]}_{\alpha_2} \quad (13)$$
$$= \left(\left(R_4 + \frac{1}{gm_4}\right) \| \frac{1}{gmf_1}\right) \alpha_2$$

$$\tau_6 = \left(\left(R_5 + \frac{1}{gm_5}\right) \| \frac{1}{gmf_2}\right) \underbrace{\left[C_{s6} + C_{gs7} + (1 + gm_7 R_7) C_{gd7}\right]}_{\alpha_3} \quad (14)$$
$$= \left(\left(R_5 + \frac{1}{gm_5}\right) \| \frac{1}{gmf_2}\right) \alpha_3$$

$$\tau_{eq} = \left(R_F \| \frac{1}{gm_3}\right)\left(\left(R_4 + \frac{1}{gm_4}\right) \| \frac{1}{gmf_1}\right) \quad (15)$$
$$\left(\left(R_5 + \frac{1}{gm_5}\right) \| \frac{1}{gmf_2}\right) \alpha_1 \alpha_2 \alpha_3$$

The 3-dB response of the TIORx can be obtained with τ_{eq} from $f_{3dB}=1/(2\pi\tau_{eq})$. Writing in terms of three dominant poles of TIORx, the three major poles would be $P_1=\tau_1$; $P_2=\tau_5$; $P_3=\tau_6$.

The input-referred noise of TIORx is described as follows:

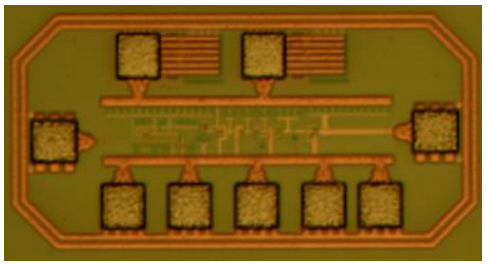
The input referred noise of Rx can be described as follows:

$$I_{n,eq} \cong I_{s1}^2 + I_{Rf}^2 + I_{R2}^2 + \left(\frac{s\left(C_{db2} + C_{gs3}\right)}{gm_3}\right)^2 \left(I_{d3}^2 + I_{R3}^2\right)$$
$$+ \left[\frac{R_1\left(1 + s\left(C_{in} + C_{gs1} + C_{sb2}\right)\right)}{\left(1 + gm_2 R_1\right) Rs}\right]^2 I_1^2$$
$$+ \left(\frac{s\left(C_{gs2} + C_{gd1}\right)}{gm_1}\right)^2 \left(I_{d2}^2 + I_{Rf}^2 + I_{R2}^2\right)$$
$$\cong 4kT\left(\frac{1}{R_{s1}} + \frac{1}{R_f} + \frac{1}{R_2}\right) + \frac{4kT\omega^2\left(C_{db2} + C_{gs3}\right)^2}{gm_3^2}$$
$$\left(\Gamma + \frac{1}{R_3}\right) + \frac{4kT\omega^2\left(C_{gs2} + C_{gd1}\right)^2}{gm_1^2}\left(\Gamma + \frac{1}{R_f} + \frac{1}{R_2}\right)$$
$$+ \frac{4kTR_1^2\left[1 + \omega^2\left(C_{in} + C_{gs1} + C_{sb2}\right)^2\right]}{\left(1 + gm_1 R_1\right)^2 R_{s1}^2}\left(\Gamma + \frac{1}{R_1}\right) \quad (16)$$

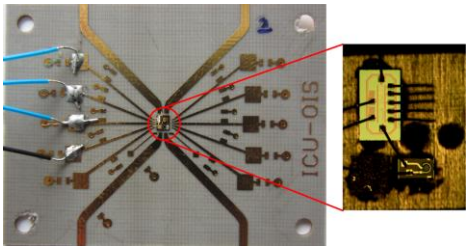
where k is Boltzmann's constant; T is the absolute temperature; Γ is the channel-noise factor of MOSFET; C_{in} is the input parasitic capacitance which includes the photodiode capacitance; bond-pad parasitic capacitance, and electrostatic discharge capacitances ($C_{in}=C_{pd}+C_{ESD}+C_{pad}$). From eq. (16), it can be observed that low frequency noise is dominated by resistor thermal noises and high frequency dominant noise occur due to input parasitic capacitances. The dominant high-frequency noise is divided by $(1+gm_1R_1)$ gain of the local feedback, and hence, the size of local feedback has been increased to reduce total equivalent noises. To reduce the noise generated from the inter-stage, the size of M_3 should be decreased to reduce its gate-source parasitic capacitance, C_{gs3}, and gm_4 should be increased as large as possible. However, increasing the size of M_4 leads to reduction in bandwidth and increase in the input-referred noise. Therefore, the inter-stage transistor sizes have to be chosen carefully not to increase the noise of TIORx or reduce bandwidth performance. Thus, the transconductance of M_3 and M_4 have been chosen to be $gm_3=2gm_4$.

III. Experimental Results

The TIORx was fabricated in a 0.13µm CMOS technology and has a core size (without pads) of 0.051mm^2. The TIORx chip is mounted on wire-bounded chip-on-board (COB) for frequency response, eye-diagram and integrated output noise measurements. The die photograph of TIORx chip and TIORx module are shown in Fig. 2. The TIORx module consists of the TIORx chip, photodiode, and 100 nF single layer capacitor connected between the PD and voltage supply to reduce the ripples from supply voltage. The transimpedance gain (Z_T) of the TIORx chip was calculated from the measured S-parameter data using an Agilent 8703B lightwave component analyzer. Frequency response is measured from 1 GHz to 16 GHz. With a 1KΩ shunt passive feedback, R_F, and 240 fF photodiode capacitance, C_{pd}, a measured transimpedance gain of 60 dBΩ with a 3-dB bandwidth of 6.9 GHz are achieved for the TIORx chip, as shown in Fig. 3.



(a)



(b)

Fig. 2. (a) Die photograph of the fabricated TIORx chip, and (b) TIORx module.

Fig. 4 shows the integrated output noise measured from the output of the TIORx chip with no input connected. The standard deviation of 0.52 mV and by subtracting the oscilloscope noise of 0.1 mV, the corrected integrated noise is 0.42 mV. Fig. 5 shows the graph of input-referred noise based on equation in [8] and measurement data. The estimated noise at 3-dB is 21pA/√Hz.

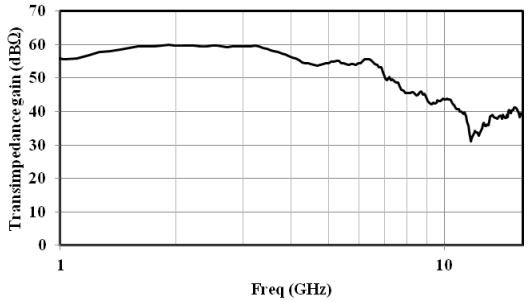


Fig. 3. The measured Z_T (dBΩ) of the proposed TIORx chip.

A 3-dB bandwidth of 6.9 GHz was obtained for the TIORx module as shown in Fig. 6. The eye-diagram have been measured using Anritsu MP1736 pulse-pattern generator with 2^{31}-1 pseudorandom binary sequence input signal, and Agilent 8610A oscilloscope. The eye-diagram is shown in Fig. 7 for the TIORx module. For an applied input light power of -9dBm, an output of 60 mV was achieved for the TIORx module.

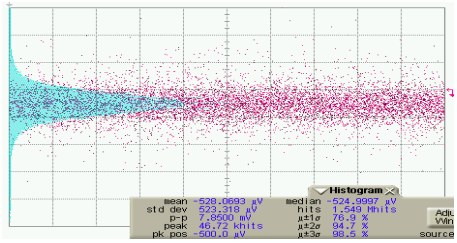


Fig. 4. Measured integrated noise output of the proposed TIORx.

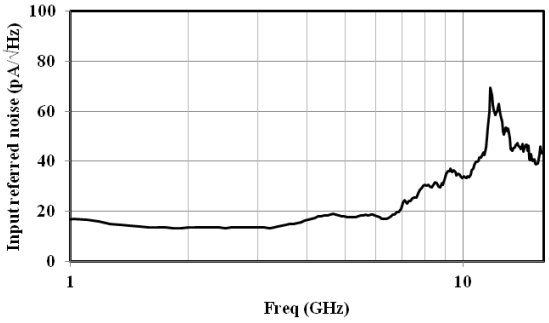


Fig. 5. The measured input-referred noise of the proposed TIORx chip.

The root-mean-sqaure (rms) jitter of 11.57 ps and rise/fall time of 86.7/85.6 ps was obtained (10% to 90%) at 10 Gbps for the TIORx module. The bit-error-rate (BER) performance of the TIORx module has been measured as shown in Fig. 8. A BER performance of less than 10^{-12} was recorded for TIORx module at 10 Gbps with -9 dBm input power. The power dissipation of the TIORx is 16.9 mW at 1.3 V of voltage supply.

TABLE I
COMPARISON OF THE PROPOSED TIA PERFORMANCE WITH OTHER WORKS

Ref.	This work	[8]	[9]	[14]	[15]	[16]
CMOS technology (µm)	0.13	0.13	0.13	0.18	0.18	0.18
Supply	1.3V	1.2V	2V	1.8	1.8	1.8
Power dissipation (mW)	16.9	4.1	98	91.8	70.2	13.97
Inductor	-	Yes	-	Yes	Yes	-
Chip core size(mm^2)	0.051	0.071	0.061	0.8	0.14	-
Data rate (Gbps)	10	10	10	10	10	10
3-dB BW (GHz)	6.9	7.5	6	7.2	7.2	8.5
Gain (dBΩ)	60	50	62	75	61	51.7
Sensitivity 10^{-12} (dBm)	-9	10 µA	22.4 µA	-18.9	10 µA	-
GBP/P_{DC}	408	578	78	441	114	234

Gain bandwidth product per DC power (GHz Ω/P_{DC}), bandwidth (BW).

Table I shows a comparison of the TIORx performance with other works. In our proposed TIORx, a relatively high gain-bandwidth product per DC power (GBP/P_{DC}) of 408 GHzΩ/mW is achieved, compared to the state of the art TIAs. In our proposed design, the addition of inter-stage and post amplifying transconductance stages increases the total noise at higher frequencies. Increase in input-referred noise leads to degradation of input sensitivity. Therefore, the sensitivity in our design is slightly smaller comparing to other artworks. Our proposed TIORx module combines the gain and bandwidth improvement advantages of a conventional Rx module, while acting as a front-end amplifier for low signals from the PD. From Table I, it can also be seen that the size of the proposed TIORx is smaller than the other TIA chips. Thus, the proposed TIORx module consumes low power and occupies a small area when compared to other high data-rate Rx modules of similar CMOS technology.

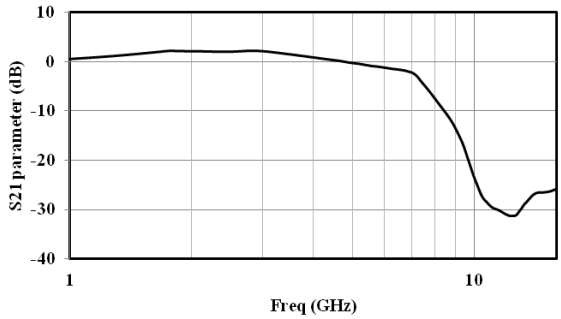


Fig. 6. Normalized S21 measurement result of the proposed TIORx module.

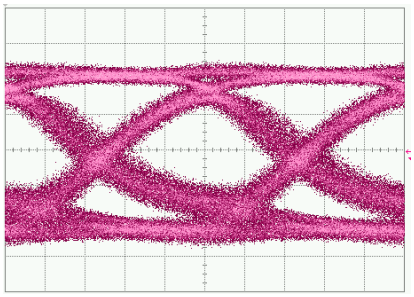


Fig. 7. Eye diagram of the TIORx module with input power of -9 dBm (62µA with 0.5 A/W responsivity of PD), 50 ps/div, 13 mV/div.

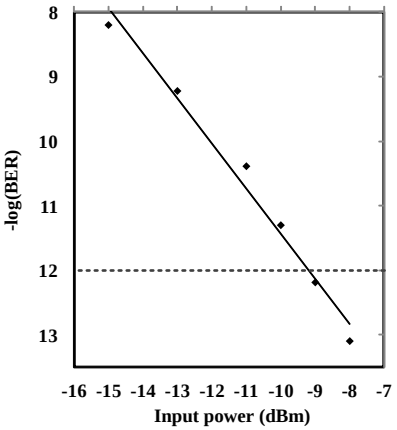


Fig. 8. BER of the proposed TIORx module at 10 Gbps.

IV. CONCLUSION

A TIORx module has been designed and fabricated in 0.13µm CMOS technology for optical interconnect applications which operates up to 10 Gbps data rate. The measured 3-dB bandwidth of the TIORx is 6.9 GHz with a transimpedance gain of 60 dBΩ. While utilizing two intersecting active feedback systems with RGC input stage, the TIORx chip core occupies a small chip area of 0.051mm^2 and has a power consumption of 16.9 mW at 1.3 V. Our proposed TIA-Rx can be applied as a front-end optical Rx to convert the input photo current to output voltage signal, high enough to feed to the next stages such as the De-serializer, PLL, and/or CDR circuits, and it is applicable for chip-to-chip optical interconnects. A GBP/P_{DC} of 408 GHzΩ/mW was achieved. The TIORx module is applicable for chip-to-chip optical interconnects.

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