A Novel Reconfigurable Architecture for Generic OFDM Modulator Based on FPGA

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***Abstract*— OFDM is a special case of multi-carrier modulations, which is of great use in various wireless communications, such as DAB, DVB, HDTV, CMMB, TMMB, 802.11a. The OFDM frame structure is similar to each other. It consists of a number of OFDM symbols following the synchronizing signal with different cyclic prefix and guard interval. In this case, it is significant for researchers to implement OFDM modulator through a novel reconfigurable architecture to meet different communication standards. This paper shows how the architecture is realized on FPGA.**

***Keywords*—OFDM, FPGA, reconfiguration, SDR, multicarrier**

I. INTRODUCTION

Orthogonal Frequency Division Multiplexing (OFDM) has been studied by researchers all over the world, which makes a great difference in modern modulate techniques. And now, it is widely used in most wireless communication systems. It is meaningful to present an architecture based on FPGA that can adapt to diverse application scenarios by simply changing the parameters of cyclic prefix and guard intervals and so on.

II. BACKGROUND

Table 1 shows several sets of OFDM parameters of different wireless application protocols.

TABLE 1. DIFFERENT OFDM PARAMETERS

Para-meters	Standards		
	CMMB (Bf = 8MHz)	**DAB (Transmission mode I)**	**DAB (Transmission mode II)**
T(us)	0.1	0.48828125	0.48828125
Tu(us)	409.6(4096T)	1000(2048T)	250(512T)
Tcp(us)	51.2(512T)	\	\
Ts(us)	460.8(4608T)	1246(2552T)	312(638T)
Tg(us)	2.4(24T)	246(504T)	62(126T)
Nv	3076	1536	384
Ns	4096	2048	512
L	53	76	76

As the difference presented in the table, we can see parameters of a specific standard vary from each other not to mention those in different ones. Particularly, DAB has no cyclic prefix, but in essence, guard interval is part of cyclic prefix. In this case, the length of cyclic prefix can be regard as long as the length of guard interval. Then, the structure of every single OFDM symbol is alike, as shown in Figure 1.

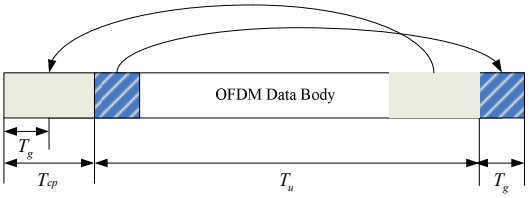

Figure 1. OFDM symbol structure

This similarity in structure makes it possible and meaningful to come up with a novel reconfigurable architecture for generic OFDM modulator. In the next section, its implementation will be discussed.

III. RTL DESIGN

This work divides the design into five main functional subsystems: constellation mapping, beacon adding, sub-carrier index, IFFT, cyclic prefix and guard interval adding and configuration.

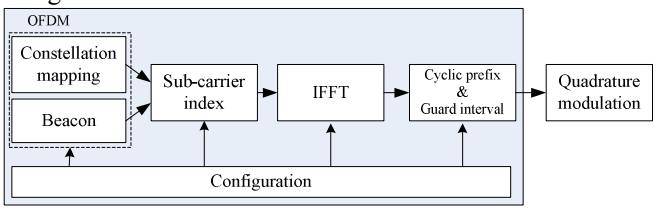

Figure 2. Block diagram

A. Constellation mapping

In this section, a number of ROMs are used to store the data of each constellation point for each specified modulation schemes (QPSK, 16-QAM, 64-QAM and so on). In terms of specific performance in different system, different precise can be choose. In general, 16-bit fixed-point data performs well in most occasions.

When configuring it to a practical modulation, the first reading address changes as well, the data read from ROM match the current modulation scheme. Figure 3 shows the structure of this module.

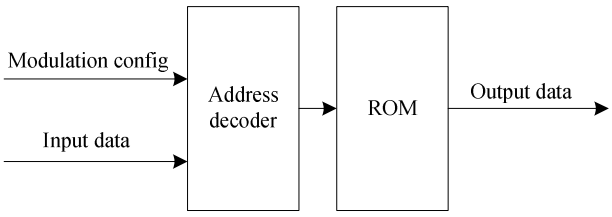

Figure 3. Diagram of constellation mapping

B. Beacon

Beacon, which is also called synchronization, consist of an identifiable sequence generated by a specific formula. It consumes a lot of resources like adders and multipliers when implementing it on FPGA. In this case, the formula is performed by Matlab and the results are stored in a specific ROM after fixed point procedure.

C. IFFT

Nowadays, Software Defined Radio (SDR) concept that focuses on flexibility on reconfiguration has been proven quite efficient, and lots of IP cores are offered by FPGA producer such as ALTERA, Xilinx and other third-party companies. To select a suitable IFFT core, several aspects must be considered, and the two most vital points of them are speed and length. It is the speed and length of IFFT that play a crucial role in the whole design defining how large the bandwidth can be achieved. Thus the IFFT core should be chosen depending on the bandwidth of system.

In different standards or different modes of a specific standard, the IFFT length also differs. More than one IFFT core can be used to solve this problem, however, this repeated work wastes lots of resources. How to use one IFFT to calculate various types of IFFT is the key point to go through.

From the FFT equations below, it is a common transformation that $x(n)$ is segmented into even and odd indexed elements. On the other hand, if the odd indexed part is set as zeros, the first half part of $X(k)$ is the result of the even indexed sequence.

$$X(m)=\sum_{n=0}^{(N/2)-1} x(2n)W_{N/2}^{nm}+W_N^m\sum_{n=0}^{(N/2)-1} x(2n+1)W_{N/2}^{nm} \quad (1)$$

$$X(m+N/2)=\sum_{n=0}^{(N/2)-1} x(2n)W_{N/2}^{nm}-W_N^m\sum_{n=0}^{(N/2)-1} x(2n+1)W_{N/2}^{nm} \quad (2)$$

$n=0,1,\cdots,(\mathrm{N}/2)-1$

$m=0,1,\cdots,(\mathrm{N}/2)-1$

$W_N=e^{-j2\pi/N}$

With another basic equation as shown in (3), IFFT calculation can also be performed by FFT.

$$x(n)=\frac{1}{N}[\sum_{k=0}^{N-1} X^*(k)W_N^{nk}]^* \quad (3)$$

Thus, an N-point IFFT can be calculated via a 2N-point IFFT core when the odd indexed part is set into zeros. Analogically, when placing the input data on $x(4n)$ where $n=0,1,\cdots,(\mathrm{N}/4)-1$, the first quarter of the results given by the 2N-point IFFT core are the desired output of N/2 points IFFT. In this case, after initializing the max IFFT length, other IFFTs whose lengths are the factors of it are also eligible to be figured out by it.

D. Sub-carrier Index

In practice, this block is processed before IFFT, which has a close connection between each other. There are always some null sub-carriers, and the positions of null sub-carriers are different. However, valid sub-carriers are sequential. In consequence, the starting and end indexes of valid sub-carriers package can be marked and stored. A counter indicating the index of the IFFT input data is generated, and after comparing it with the start and end of the package, the sub-carriers will be allocated to the right positions. One obstacle, however, is how to insert zeros into the sequence properly. To solve the problem, the input sequence must be reassembled.

Figure 4 shows the original IFFT input data sequence and the point a, b, c and d indicate the edges of the sub-carriers.

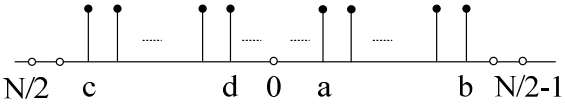

Figure 4. Original IFFT input data

After calculating N-point IFFT with a 2N-point IFFT core, the sequence should be like as shown in Figure 5.

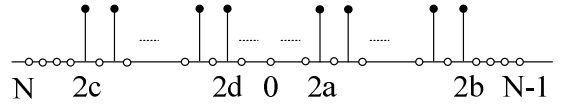

Figure 5. IFFT input data when using a 2N-point IFFT core

Because of the inserted zeros, the indexes are doubled. To avoid the change of the structure, the lowest bit of the counter will be discarded when comparing with the marked points. Of course, the lowest two bits should be deserted when realizing N/2 points IFFT via a 2N-point IFFT core.

E. Guard interval and cyclic prefix

There are various lengths of guard interval and cyclic prefix even in one given standard not to mention different standards. But for its processing similarity, it is not a necessity to realize it separately. When the IFFT output data stream arrives, a true dual port RAM of the max OFDM symbol length is used to store the data. The storage method is shown in Figure 6.

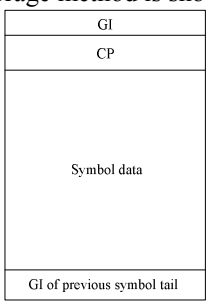

Figure 6. Storage strategy of the true dual port RAM

Another important point of the block is how to dispatch the two true interface of RAM.

As for the cyclic prefix, it is just to repeat the tail of the data body. When receiving this part of data, two ports are working simultaneously. One is for the data body orderly, while the other one is writing data from the beginning address. The timing diagram is shown in Figure 7.

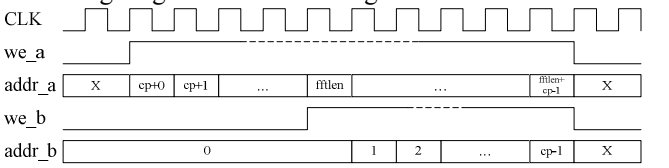

Figure 7. Timing diagram of cyclic prefix

This step fills the RAM with the original data from IFFT, and cyclic prefix has been written in the same time. Diverse lengths of cyclic prefix make no difference.

With regard to guard interval, three variables are required to calculate a single data in this section, the window parameter gi_data stored in a ROM, the current data *q_b* and the overlapping data of previous symbol q_a. Fig.8 shows this precise relationship.

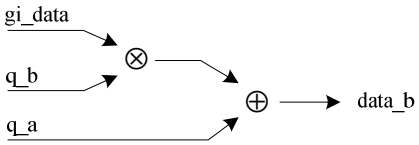

Figure 8. The operations of guard interval

Furthermore, the desired result has to be written back into the RAM after all the operations, and current overlapping GI data has to be calculated. Obviously, two ports can not accomplish this all at one time, taking other data processes like rounding off into account, 8 clocks are taken to arrange the pipeline. Table 2 shows the pipeline clearly.

TABLE 2. PIPELINE STAGE

Cycle	Signals		
0	addr_b	gi_addr	addr_a
1	q_b	gi_data	q_a
2	mult_rb mult_ib	mult_ra mult_ia	
3	mult_real	mult_imag	
4	mult_real_reg	mult_imag_reg	
5	sum_real	sum_imag	
6	data_b_reg		
7	data_b		

F. Configuration

Since the storage space and IFFT length are designed according to their maximum, FPGA should be informed of current processing length.

This part provides all the parameters to all the sections above, including the choice between synchronizing signal and ordinary signal, the position where zeros are inserted, the indexes of the edge of the sub-carriers, the length of IFFT, cyclic prefix and guard interval. Exact parameters which are needed to be configured are shown in Figure 9.

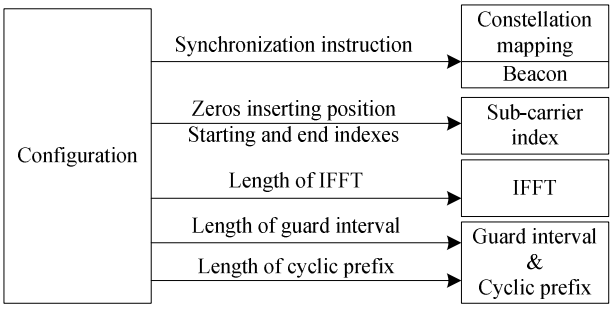

Figure 9. Configurated parameters

IV. RESULTS

After the implementation of the model, different parameters from different standards in Table 1 are configured. The whole design runs on the DE2-115 development board from ALTERA, which use EP4CE115F29C7 as the main processing chip. And the resource consumption is shown in Table 3.

TABLE 3. SPEED AND AREA RESULTS

Parameters	Used		
	CMMB	DAB (mode I)	DAB (mode II)
Number of M9Ks	51	38	38
Number of DSP18*18	26	26	26
Number of LEs	11078	10853	10853
Symbol rate(MSPS)	10	2.048	2.048

When used in CMMB system, more M9Ks and LEs are needed because the max IFFT length is 4096. While these two modes of DAB have the same resource consumption for they are designed based on max storage space and IFFT length.

While running on the development board, several spectrum graphics were captured on spectrum analyzer.

Figure 10 shows the spectrum of CMMB when bandwidth is 8MHz.

Figure 11 shows another sort of spectrum of digital radio. As a result of configuring variable start index and end index of package, upper half-sub-band and lower half-sub-band are located on opposite sides of the center frequency, which is beneficial to retain compatibility with existed wireless communication system and increase spectrum efficiency.

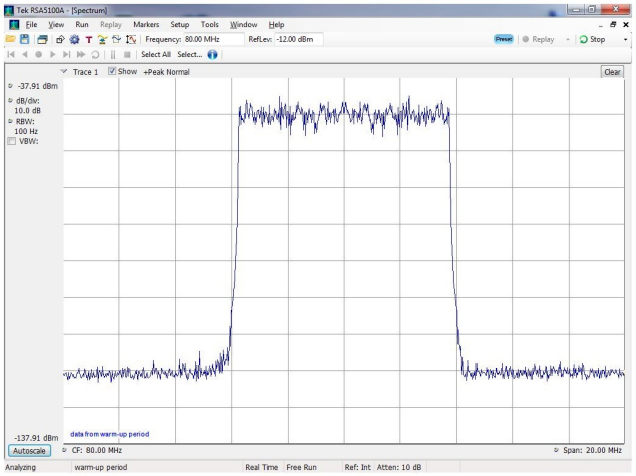

Figure 10. Spectrum of CMMB

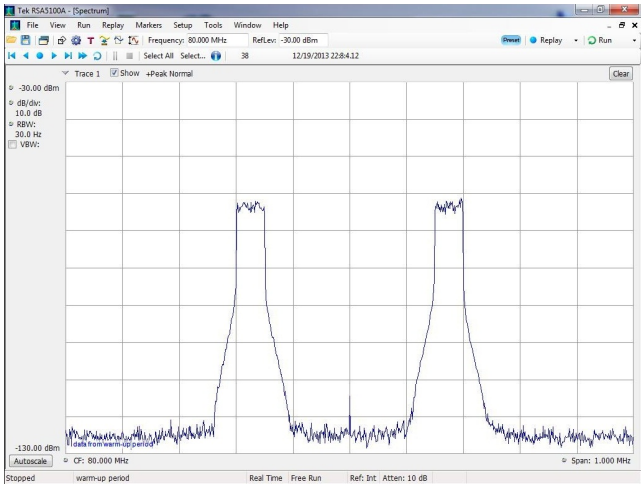

Figure 11. A special spectrum of digital radio

V. CONCLUSION

It has been presented that the complete design can fit for OFDM modulators of different wireless standards with different IFFT length, sub-carrier index, cyclic prefix and guard interval, whose resource consumption is quite low as well.

Also, implementing this work on FPGA indicates that the SDR concept can be realized on current ordinary devices like Cyclone IV series. Reducing repetitive work makes the system design more convenient and efficient.

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