A 1.8 V-to-2.5 V MIPI RFFE Slave Interface CMOS Circuit

Seunghyun Jang*, Namsik Ryu, Hui Dong Lee, Bonghyuk Park
ETRI (Electronics and Telecommunications Research Institute)
Gajeong-ro 218, Yuseong-gu, Daejeon, South Korea
damduk@etri.re.kr*

Abstract—The MIPI RFFE slave interface circuit including Power-on-Reset (PoR), SCLK receiver and SDATA bi-directional transceiver has been implemented with a CMOS 250 nm process. Simulation results show that the designed circuit has SDATA output transition time (for rise and fall) of shorter than 3.3 ns at a full-speed rate of 26 MHz, which satisfies the timing requirement (< 6.5 ns) by the specification of MIPI RFFE version 1.10. The target load capacitance that the designed MIPI RFFE slave interface circuit drives is 26 pF for the configuration of one master and eight slaves.

Keyword—MIPI, RFFE, master, slave, PoR, SCLK, SDATA, CMOS, driver

Seunghyun Jang received the B.S. degree from Inha University, Incheon, Korea in 2001, in the Department of Electrical, Electronic Engineering and Computer Science, and the M.S. degree from Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Korea in 2003. Following graduation, he joined Electronics and Telecommunications Research Institute (ETRI), Daejeon, Korea. His research experiences include wideband VGAs for UWB CMOS RF transceiver, supply modulators for an envelope-tracking power amplifier and continuous-time delta-sigma modulators. His current research focus is on highly efficient power amplifiers and mixed-signal circuits for them.