Reconfigurable Network Accelerator for Wireless Sensor Nodes

Wei LIU [a], Zhengqiang WANG [a], Shaohua QU [a], Rong LUO [b]

[a] Department of Physics & Electronic Engineering, Hubei University of Arts and Science, China

[b] Office of Scientific Research and Development, Tsinghua University, China

13911622678@163.com, 283724532@qq.com, 455095579@qq.com, luorong@tsinghua.edu.cn

Abstract— **Power consumption is one of the most critical challenges in wireless sensor networks, as sensor nodes are powered by batteries in most situations. Wireless communication is the main source of power consumption in a sensor node. Many energy aware protocols and algorithms have been proposed in the past few years. The basic idea of these methods is to reduce the data that nodes exchange and the time that nodes work. These methods are mostly software based, so microcontrollers are responsible for performing them. However, they are not efficient enough to interact with the communication hardware. In this paper, a flexible network accelerator is proposed. It is hardware based and reconfigurable, so it can interact with the communication hardware more efficiently and reduce power consumption further. Three modes are designed for this network accelerator: Full Software Mode, Partial Acceleration Mode and Full Acceleration Mode. These modes are suitable for different application requirements. Design details are described for these modes. We prototype this network accelerator using a traditional mote and a CPLD board. Preliminary results show it is feasible and more than 90% energy consumption can be reduced.**

Keywords— **Wireless Sensor Node, Architecture, Network Accelerator, Reconfigurable, CPLD**

I. INTRODUCTION

In recent years, wireless sensor networks have developed from academic research hotspots to a technology that is being deployed in numerous application areas such as environmental monitoring, industrial control, and home automation. These networks are composed of hundreds and thousands of low cost, low power and miniaturized sensor nodes, which are densely deployed in target areas and cooperate to complete particular tasks. Typically, sensor nodes are powered by batteries and recharging or replacing these batteries for so many nodes is infeasible or even impossible in certain cases. As a result, power consumption becomes one of the most critical challenges in wireless sensor networks.

Wireless communication is the main source of power consumption in a sensor node. To maximize the lifetime of wireless sensor networks, many energy aware protocols and algorithms have been proposed in the past few years [1]. The basic idea of these methods is to reduce the data that nodes exchange and the time that nodes work. These methods are mostly software based, so microcontrollers are responsible for performing them. However, as microcontrollers are always designed and optimized for general-purpose tasks, they are not flexible and efficient enough to interact with the underlying communication hardware.

To solve these drawbacks, new sensor node architectures based on reconfigurable hardware are proposed in recent years [2]. Reconfigurable hardware are used to process tasks that microcontrollers are not good at. For example, as processing capabilities of microcontrollers are very limited, it is time consuming to perform computing intensive tasks. However, these tasks can be processed more efficiently in reconfigurable hardware, because special design and optimization could be down for them.

In this paper, a hardware-based and reconfigurable network accelerator is proposed. It is invented to interact with the communication hardware more efficiently. This network accelerator takes characteristics of wireless communication and networking in wireless sensor networks into account. As a result, it can reduce power consumption further. The main contributions of our work includes two aspects: First, general framework for network acceleration is proposed and three modes for different application requirements and sensor platforms are designed. Second, a prototype is implemented and preliminary results are analysed.

The rest of this paper is organized as follows. In Section II, related works of sensor node architecture are discussed. In Section III, the proposed network accelerator is described and three different modes are explained. Section IV shows the prototype implementation and preliminary results. We conclude this paper in Section V.

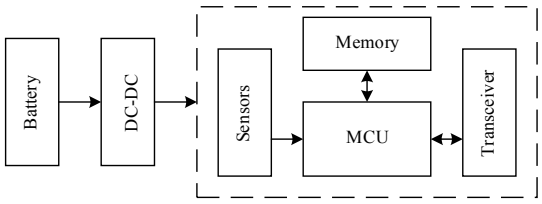

Figure 1. Traditional Sensor Node Architecture

II. RELATED WORKS

Traditional wireless sensor nodes consist of four subsystems [3]: a microcontroller with memory, a transceiver, some sensors and an energy source, as shown in Figure 1. This

architecture, developed by researchers from University of California, Berkeley, is the de facto standard for wireless sensor node. Two most popular platforms of this architecture are MicaZ [4] and TelosB [5], which have been the foundation for hundreds of research works around the world. Specifications of these platforms are listed in Table 1. These platforms are based on 8bit or 16bit general purpose microcontrollers and suffer from low flexibility. They are not good at processing tasks related to data analysis and complicated network protocols. For example, it is very difficult to perform encryption and decryption with such microcontrollers [6].

TABLE 1. SPECIFICATIONS OF MICAZ AND TELOSB

Platform	Specification		
MicaZ	MCU	Type	ATmega128L
		Clock Frequency	7.3728MHz
		Flash/RAM/EEPROM	128KB/4KB/4KB
		Active Current	8mA
		Sleep Current	< 15uA
	Radio	Type	CC2420
		Frequency Band	2.4GHz ISM
		Data Rate	250kbps
		Transmit Power	-24dBm~0dBm
		Max TX Current	17.4mA
		RX Current	19.7mA
		Idle/Sleep Current	20uA/1uA
TelosB	MCU	Type	MSP430F1611
		Clock Frequency	8MHz
		Flash/RAM/EEPROM	48KB/10KB/16KB
		Active Current	1.8mA
		Sleep Current	5.1uA
	Radio	Type	CC2420
		Frequency Band	2.4GHz ISM
		Data Rate	250kbps
		Transmit Power	-24dBm~0dBm
		Max TX Current	NA
		RX Current	23mA
		Idle/Sleep Current	21uA/1uA

As power consumption of programmable logic devices, such as FPGAs and CPLDs, continue to reduce with the improvements of semiconductor technology, they begin to be used to build sensor nodes. CPLDs are suitable for simple applications while FPGAs are useful for complex ones. Their reconfigurable ability gives sensor nodes more flexibility.

Authors in [7] design Cyclops sensor node for image sensing and interpretation. A Xilinx CPLD is used to provide low power consumption. This architecture is mainly for higher level image processing algorithms. In [8], the authors propose a rapidly reconfigurable miniature sensor node with a low-power Actel Flash FPGA. They implement a transport triggered architecture processor in this node. The implemented processors and algorithms are intended for rolling bearing condition monitoring. However, in these works, reconfigurable devices are used to perform complex computation tasks, not for communication tasks.

Mplemenos et al [9]-[11] use reconfigurable hardware devices in WSNs for accelerating complex communication tasks and reducing power consumption. In [9], they use Xilinx CPLD to accelerate the Cost Estimation algorithm of the XMesh routing protocol. In [10], they use Xilinx CPLD to accelerate the Cost Estimation algorithm and the Blowfish encryption algorithm. In [11], they use Xilinx FPGA to accelerate the greedy perimeter stateless routing protocol. As they claim, significant energy conservations can be achieved using reconfigurable devices. However, in these works, reconfigurable devices are used as a separate coprocessor to accelerate particular protocols and algorithms.

PowWow [12] is a similar node architecture compared with ours. It introduces Actel FPGA for low layer processing of packets. This architecture is used to accelerating CRC32 algorithm for error detection. However, it isn't a general framework for network acceleration and cannot satisfy requirements for different application and sensor platforms.

III. SYSTEM ARCHITECTURE

A. New Sensor Node Architecture with CPLD

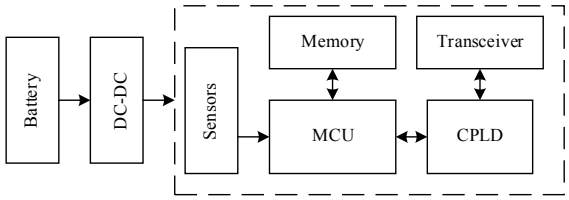

Figure 2. New Sensor Node Architecture with CPLD

In this paper, we propose a general framework for reconfigurable network accelerator. To accommodate this network accelerator, new sensor node architecture is designed, as shown in Figure 2. In this architecture, Transceiver is no longer connected to MCU directly. Instead, CPLD is used to bridge MCU and transceiver. CPLD is selected here because it's more efficient in terms of power consumption and performance.

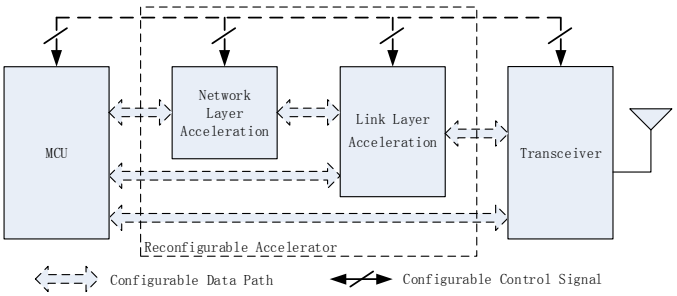

Figure 3. Architecture for Network Accelerator

B. Architecture for Network Accelerator

The general framework for proposed reconfigurable network accelerator is illustrated in Figure 3. According to different application requirements and sensor platforms, the accelerator can be configured in different modes. For example, routing and forwarding features of network layer could be implemented in the accelerator, while other features could be

persisted in MCU or transceiver. Three modes are designed for this framework: Full Software Mode, Partial Acceleration Mode and Full Acceleration Mode.

C. Different Modes for Accelerating

As sensor networks can be used in huge variety of applications and these applications need different sensor platforms with heterogeneous computation and communication abilities, there is no changeless network acceleration architecture. This is exactly why we need a reconfigurable network accelerator. To accommodate for this, we designed three different modes for this framework.

1) *Full Software Mode*: Full software mode is fully compatible with traditional sensor node architecture where transceiver is connected to MCU directly, as shown in Figure 4. In this mode, network protocols are implemented in two ways: First, if transceiver doesn't provide hardware support, such as CC1000 used in Mica2 [13], the protocols of all layers are implemented in software by MCU. Second, if transceiver provide some hardware support, such as CC2420 used in MicaZ, reminder protocols are implemented in software by MCU.

In this mode, CPLD is just used to hard wire the data and control signals of MCU and transceiver together. As it doesn't need any dynamic operations, the power consumption increased by CPLD can be negligible.

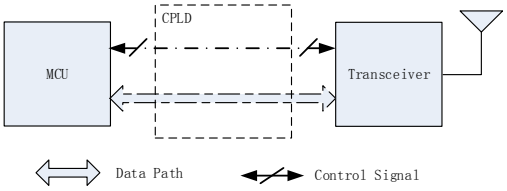

Figure 4. Full Software Mode

2) *Partial Acceleration Mode:* Partial Acceleration Mode is used to accelerate key algorithms which are not efficient when implemented by MCU, as shown in Figure 5. In this mode, most network tasks are still performed by MCU. CPLD is used as a coprocessor. For example, encryption and decryption can be implemented by CPLD instead of MCU to reduce execution time and power consumption.

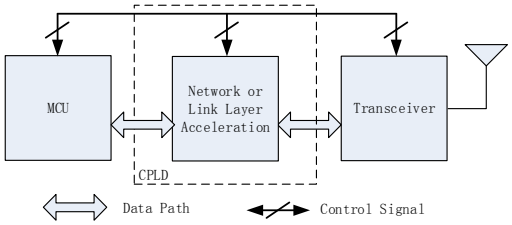

Figure 5. Partial Acceleration Mode

3) *Full Acceleration Mode:* Some applications require parallelism between processing and communication. For example, structural health monitoring applications need high speed sampling synchronously among multiple nodes. If it is interrupted by communication tasks, such as forwarding packets for other nodes, synchronous sampling may be affected and sampled data becomes useless. This parallelism can be achieved by full acceleration mode, as shown in Figure 6. In this mode, basic networking features are implemented in CPLD, such as lookup the next hop node, media access control, and interfacing the underlying transceiver. When MCU finishes configuring the network accelerator, it can dedicate to perform processing tasks, without disturbing by communication tasks.

At the other hand, when there is no processing tasks, the MCU can be put in deep sleep mode to preserve energy. It can be waked up by the network accelerator only when a packet destined for this node is received and has to be processed by application layer, or by the sensors when important events appear. As CPLD is more efficient than MCU when performing simple packet forwarding tasks, energy consumption will be reduced significantly.

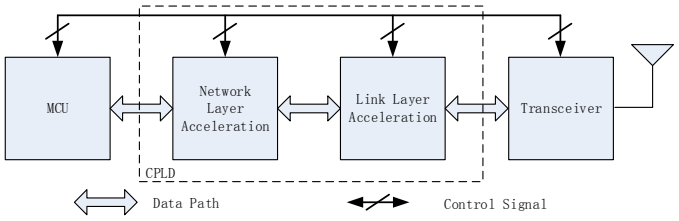

Figure 6. Full Acceleration Mode

IV. Prototype Implementation

To validate and evaluate the sensor node architecture and network accelerator we proposed, a prototype is implemented. The MCU and transceiver of MicaZ node are selected because MicaZ is one of the most popular sensor platforms. In this way, experimental results can be compared with MicaZ to illustrate the advantages of our proposed architecture.

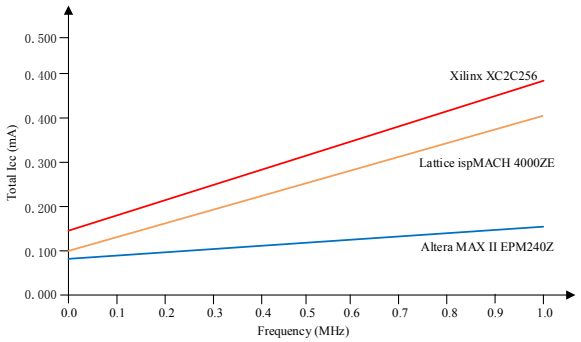

Figure 7. Dynamic current for three popular CPLD

A. Selection of the CPLD

The crucial component in our architecture is the CPLD. Static and dynamic power consumption of the CPLD are the most important parameter affecting our choice. Figure 7 illustrates the dynamic current of the Altera MAX IIZ CPLD compared with a Xilinx CoolRunner-II macrocell based CPLD and Lattice ispMACH 4000ZE CPLD. It is shown that MAX

IIZ CPLD provides significantly lower current at every performance level. So we choose Altera MAX IIZ CPLD to implement our prototype.

B. Hardware Design

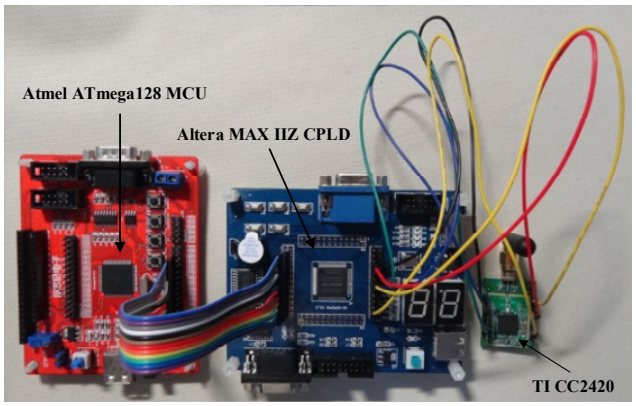

Figure 8. Hardware Design

To compare with MicaZ, our prototype is consisted of an Atmel ATmega128 development board, an Altera MAX IIZ CPLD development board, and a TI CC2420 transceiver module, as shown in Figure 8. For MCU, we use Atmel Studio 6.2 to develop and program [14]. For CPLD, we employ Quartus web 14.1.0 for synthesis and route, while ModelSim Altera edition is used for logic and timing simulation [15].

C. Preliminary Results

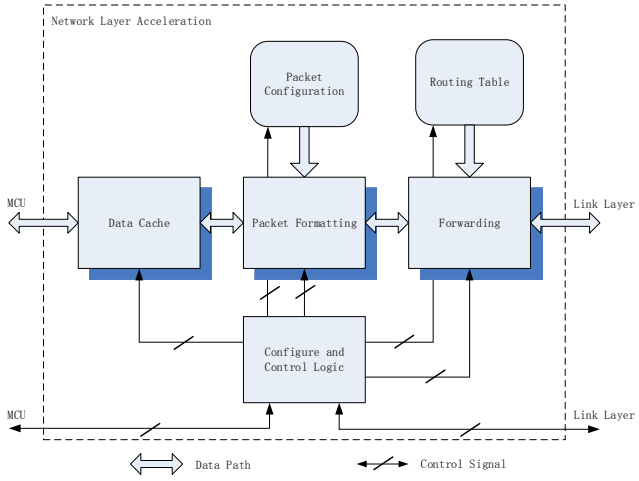

Figure 9. Network Layer Acceleration

As CC2420 is a packet level transceiver and provides some hardware support for link layer protocol, we use this prototype to implement simple network layer acceleration in order to evaluate its efficiency. The features for network layer acceleration is shown in Figure 9. A routing table is configured by MCU when routing protocol is done. Then the network accelerator could run independently until new routing information has to be updated. When compared with MicaZ that implements the same function, more than 90% energy consumption can be reduced.

V. Conclusions

As sensor nodes are powered by batteries, prolonging their lifetime is one of the most critical challenges in wireless sensor networks. Traditional sensor node architecture based on general purpose microcontrollers is not efficient and flexible enough to minimize power consumption. In this paper, a new sensor node architecture based on reconfigurable network accelerator is proposed. This network accelerator takes characteristics of wireless communication and networking in wireless sensor networks into account. Three modes are designed for this network accelerator: Full Software Mode, Partial Acceleration Mode and Full Acceleration Mode. These modes are suitable for different application requirements. Preliminary results show it is feasible and more than 90% energy consumption can be reduced. In the future, detailed performance tests will be conducted and integrated node platform will be implemented. With the integrated platform, their performance in realistic network environments will be evaluated.

Acknowledgment

This work is partially funded by Foundation of Hubei Provincial Department of Education under grant number 2012362 and Foundation of Xiang Yang Science and Technology Bureau under grant number 2014[12].

References

[1] N. A. Pantazis, S. A. Nikolidakis, and D. D. Vergados, "Energy-efficient routing protocols in wireless sensor networks: a survey," *IEEE Communications Surveys & Tutorials*, vol. 15, pp. 551-591, May. 2013.
[2] F. Karray, M. W. Jmal, M. Abid, M. S. BenSaleh, and A. M. Obeid, "A review on wireless sensor node architectures," in *Proc. ReCoSoC'14*, 2014, p. 1.
[3] V. Raghunathan, C. Schurgers, S. Park, and M. B. Srivastava, "Energy-aware wireless microsensor networks," *IEEE Signal Processing Magazine*, Vol. 19, pp. 40-50, Mar. 2002.
[4] "MicaZ data sheet," MEMSIC, Andover, USA.
[5] "TelosB data sheet," MEMSIC, Andover, USA.
[6] W. Liu, R. Luo, and H. Z. Yang, "Cryptography overhead evaluation and analysis for wireless sensor networks," in *Proc. CMC'09*, 2009, p. 496.
[7] M. Rahimi, R. Baer, O. I. Iroezi, J. C. Garcia, J. Warrior, D. Estrin, M. Srivastava, "Cyclops: in situ image sensing and interpretation in wireless sensor networks," in *Proc. SenSys'05*, 2005, p. 192.
[8] T. Nylanden, J. Boutellier, K. Nikunen, J. Hannuksela, and O. Silven, "Reconfigurable miniature sensor nodes for condition monitoring," in *Proc. SAMOS'12*, 2012, p. 113.
[9] G. G. Mplemenos, P. Christou, and I. Papaefstathiou, "Using reconfigurable hardware devices in WSNs for accelerating and reducing the power consumption of header processing tasks," in *Proc. ANTS'09*, 2009, p. 1.
[10] G. G. Mplemenos, P. Christou, and I. Papaefstathiou, "Using reconfigurable hardware devices in WSNs for reducing the energy consumption of routing and security tasks," in *Proc. GLOBECOM'10*, 2010, p. 1.
[11] G. G. Mplemenos, and I. Papaefstathiou, "Fast and power-efficient hardware implementation of a routing scheme for WSNs," in *Proc. WCNC'12*, 2012, p. 1710.
[12] O. Berder and O. Sentieys, "PowWow: power optimized hardware/software framework for wireless motes," in *Proc. ARCS'10*, 2010, p. 1.
[13] "Mica2 data sheet," MEMSIC, Andover, USA.
[14] The Atmel website. [Online]. Available: http://www.atmel.com/.
[15] The Altera website. [Online]. Available: http://www.altera.org/.

Wei Liu was born in Jinan, China, on January 21, 1981. He received his B.E. degree in Information Engineering from Southeast University in 2003 and Ph.D degree in Electronic Science and Technology from Tsinghua University in 2009. He is currently an adjunct professor in Hubei University of Arts and Science. His research interests include wireless communication, wireless sensor networks, embedded systems.

Zhengqiang Wang received the B.SC degree in Physics from Kashgar Teacher's College in 1996 and M.S. degree in Circuits and Systems from Central China Normal University in 2006. He is currently a professor in Hubei University of Arts and Science. His research interests include communication signal processing and wireless mesh networks.

Shaohua Qu received the B.SC degree in Physics in 1990 and Ph.D degree in Circuits and Systems in 2008, both from Huazhong University of Science and Technology. He is currently a professor in Hubei University of Arts and Science. His research interests include sensor technology, wireless sensor networks and Digital signal processing.

Rong Luo received her double B.S degree in Engineering Physical and Electronic Engineering and the Ph.D degree from Tsinghua University in 1992 and 1997, respectively. Currently, she is an associate professor at the Office of Scientific R&D, Tsinghua University. Now, her research work is mainly on Digital System Design Technology.