A High-Performance Parallel Computation Hardware Architecture in ASIC of SHA-256 Hash

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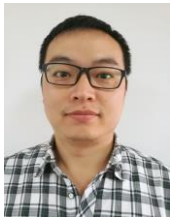
***Abstract*—The SHA-256 is playing an important role in various applications, such as e-transactions and bitcoins. To achieve more profits, the SHA-256 computation capacity is a main research direction of Hashing Algorithm. In this paper, a high-performance hardware architecture of SHA-256 hash is proposed. The computation of SHA-256 is rescheduled based on hardware characterises. Three pipelines are used to replace the critical path in the round functions which can shorten the long critical path, and divide the computation chain into independent parts. Multi-computation of SHA-256 is working in parallel pipelines, indicating that the computation capacity can be 3 times of standard SHA-256 implementation. The proposed SHA-256 hardware architecture has been implemented and synthesized with Intel 14nm technology. Simulation and synthesis results show the proposed SHA-256 hashing throughput can be improved by 3 times with 50.7% power reduction, at an area cost of 2.9 times compared to the standard implementation.**

***Keyword*—About Cryptography; Application specific integrated circuits; High-speed integrated circuits; Low-power**



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