

# A High Throughput and Flexible Rate 5G NR LDPC Encoder on a Single GPU

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**Abstract**—In order to build a high-performance low-density parity-check (LDPC) communication link simulation platform, high speed LDPC encoding for information sequence is required. In this paper, a high and flexible throughput LDPC encoding implementation based on a single GPU is proposed. We discuss the parallelism of the LDPC encoding algorithm employs the core parity check bits and single diagonal parity check bits for the fifth-generation new ratio. We implement the parallel LDPC encoder on CUDA platform. The experimental results show that our LDPC encoding module achieves a 38–62Gbps throughput for the rate from 1/2 to 8/9 on a single GPU. The results also demonstrate that parallel simulation tasks based on GPUs can achieve a good trade-off between performance and cost.

**Keyword**—5G New Ratio, quasi-cyclic LDPC code, channel encoding, parallel computing, CUDA



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