# Optimizing Implementation of SNN for Embedded System

Hyeonguk Jang, Jae-Jin Lee, Kyuseung Han

Electronics and Telecommunications Research Institute, Daejeon, 34129, Korea

**lemon@etri.re.kr, ceicarus@etri.re.kr, han@etri.re.kr**

*Abstract*— **Spiking neural networks (SNNs) are a highly promising AI technology for embedded systems, owing to their energy-efficient properties. However, the manual implementation of SNNs encounters practical challenges because of the all-to-all connections in large networks. Thus, this paper presents a novel methodology to reduce wire congestion in the SNN implementations while mitigating adverse effects on inference accuracy.**

*Keyword*— **back propagation through time, deep learning, embedded system, hardware, spiking neural networks**

**Hyeonguk Jang** received his B.S. and M.S. degrees in electrical engineering from Gyeongsang National University, Jinju, South Korea, in 2013 and 2015, respectively, and his Ph.D. degree in ICT from the University of Science and Technology, Daejeon, South Korea in 2021. He is currently working at Electronics and Telecommunications Research Institute, Daejeon, South Korea, as a post doctor. His interests include spiking neural network, deep neural network and design of RISC-V based low-power embedded systems.

**Jae-Jin Lee** received the B.S., M.S., and Ph.D. degrees in computer engineering from Chungbuk National University, Cheongju, South Korea, in 2000, 2003, and 2007, respectively. He is a leader of the AI Edge SoC Research Section, Electronics and Telecommunications Research Institute, Daejeon, South Korea. His research interests include spiking neural network and RISC-V based embedded systems.

**Kyuseung Han (Member, IEEE)** received the B.S. and Ph.D. degrees in electrical engineering and computer science from Seoul National University (SNU), Seoul, South Korea, in 2008 and 2013, respectively. Since 2014, he has been with the Electronics and Telecommunications Research Institute, Daejeon, South Korea. His current research interests include reconfigurable architecture, network-on-chip and computer-aided design of low-power embedded systems.