

Optimized Min-Sum Decoding Algorithm for Low Density PC Codes

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Abstract— Low Density Parity Check (LDPC) approaches Shannon limit performance for binary field and long code lengths. However performance of binary LDPC code is degraded when the code word length is small. An optimized min-sum algorithm for LDPC code is proposed in this paper. In this algorithm unlike other decoding methods an optimization factor has been introduced in both check node and bit node of the Min-sum algorithm. The optimization factor is obtained before decoding program and the same factor is multiplied twice in one cycle. So the increased complexity is fairly low. Simulation results show that the proposed Optimized Min-Sum decoding algorithm performs very close to the Sum-Product decoding, while preserving the main features of the Min-Sum decoding, that is low complexity and independence with respect to noise variance estimation errors.

Keywords— LDPC codes, Min-sum algorithm, Normalized min-sum algorithm, Optimization factor.

I. INTRODUCTION

Among the error correction codes Low Density Parity Check (LDPC) is one of the most efficient techniques. It was first introduced by Robert Gallager in 1962 in his PhD. dissertation [1]. It is the extreme sparseness of the parity check matrix for LDPC codes that makes the decoding particularly attractive. LDPC codes have recently received a lot of attention because they can achieve a remarkable performance near Shannon limit over the binary symmetric channel (BSC) as well as the additive white Gaussian noise (AWGN) channel [2]. The decoding of an LDPC code allows a high degree of parallelism, which makes it very suited for high data rate applications such as wide-band wireless multimedia communications and magnetic storage systems [3], [4]. The low-density nature of the parity check matrix thus, contributes both to good distance properties and the relatively low complexity of the decoding algorithm [5]. Well-designed

irregular LDPC codes demonstrate better performance than regular ones [6]. Among a variety of decoding algorithms, the well-known Sum Product (SP) algorithm [7] achieves a good decoding performance but requires a large hardware complexity. There are alternative methods such as several kinds of Min-Sum (MS) algorithms which can significantly reduce the hardware complexity of SP at the cost of acceptable performance degradation, where complex computations at the check nodes are approximated by using simple comparison and summation operations. Recently, the modified MS algorithms using correction factors have been preferred for many practical applications since they offer comparable decoding performance compared to that of SP [7] for regular LDPC codes [8], [9]. Also, for irregular LDPC codes, the improved normalized or offset MS algorithms exhibit small performance degradations [10], [11]. Specifically, the offset MS algorithm has been implemented for several practical applications due to its better performance and simple computations.

The main decoding algorithms of LDPC codes include soft-decision such as Sum Product (SP) algorithm [7] and hard-decision such as Bit flipping. In iterative decoding, a critical tradeoff between "complexity" and "performance" is required. Based on these two issues, LDPC codes may be classified as optimal, sub-optimal or quasi-optimal. The optimal iterative decoding is performed by the Sum-Product algorithm [7] at the price of an increased complexity, computation instability, and dependence on thermal noise estimation errors. The Min-Sum algorithm [12] performs a suboptimal iterative decoding, less complex than the Sum-Product decoding. The sub-optimality of the Min-Sum decoding comes from the overestimation of check-node messages, which leads to performance loss with respect to the Sum-Product decoding. Several correction methods were proposed [13-15] in the literatures in order to recover the performance loss of the Min-Sum decoding with respect to the Sum-Product decoding. We call such algorithms quasi-optimal. An example is Normalized min-sum algorithm proposed by Chen and Fossorier [16]. In this paper we propose an optimized min sum algorithm which has better performance not only from min sum algorithm but also from normalized min sum algorithm.

The rest of the paper is organized as follows. In section II, different LDPC decoding algorithms are discussed and section III explains our proposed Optimized Min-sum algorithm. Section IV discusses the simulation results and finally section V concludes the paper.

II. LDPC DECODING ALGORITHM

Decoding of LDPC codes can be two types: hard decision decoding and soft decision decoding

Hard Decision Decoding

For each bit c_n , compute the checks for those checks that are influenced by c_n . If the number of nonzero checks exceeds some threshold (say, the majority of the checks are nonzero), then the bit is determined to be incorrect. The erroneous bit is flipped and correction continues. This simple scheme is capable of correcting more than one error. Suppose that c_n is in error and that other bits influencing its checks are also in error. Arrange the Tanner graph with c_n as a root considering no cycle in the graph. In Fig. 1, suppose the bits in the shaded boxes are in error. The bits that connect to the checks connected to the root node are said to be in tier 1. The bits that connect to the checks from the first tier are said to be in tier 2. Then, decode by proceeding from the “leaves” of the tree (the top of the figure). By the time decoding on c_n is reached, other erroneous bits may have been corrected. Thus bits and checks which are not directly connected to c_n can still influence c_n .

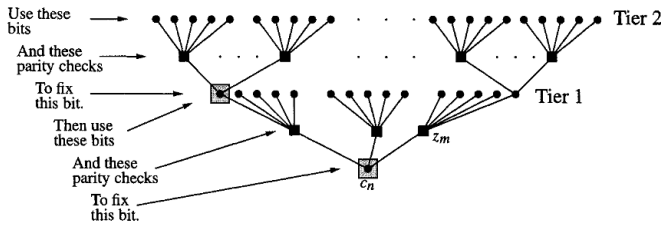


Figure 1. A parity check tree associated with the Tanner graph [18]

Soft Decision Decoding

In the Soft decision decoding, rather than flipping bits (a hard operation), we propagate probabilities through the Tanner graph, thereby accumulating evidence that the checks provide about the bits. The optimal (minimum probability of decoding error) decoder seeks a codeword $\hat{c}$ which maximizes $P(c|r, A\hat{c}=0)$. So, it seeks the most probable vector which satisfies the parity checks, given set of received data $r = [r_1, r_2, \dots, r_N]$. However, the decoding complexity

for the true optimum decoding of an unstructured (i.e., random) code is exponential in K , requiring an exhaustive search over all 2^K codewords. Instead, the decoder attempts to find a codeword having bits c_n which maximize $P(c_n|r, \text{all checks involving bit } c_n \text{ are satisfied})$, it is the posterior probability for a single bit given that only the checks on that bit are satisfied. As it turns out, even this easier, more computationally localized, task cannot be exactly accomplished due to approximations the practical algorithm must make. However, the decoding algorithm has excellent demonstrated performance and the complexity of the decoding is linear in the code length.

LDPC decoding is based on the parity check matrix which can also be represented using a bipartite graph. Columns in the parity check matrix represent variable nodes and rows in the matrix represent check nodes. Each variable node corresponds to one bit of the codeword and each check node corresponds to one parity check equation. Edges in the graph connect variable nodes to check nodes and represent the nonzero entries in H matrix. The term “low density” conveys the fact that the fraction of nonzero entries in H is small, in particular it is linear in the block length n . Parity check matrix can be of regular and irregular types. In this paper we use the regular codes. For regular codes, the corresponding H matrix has d_c ones in each row and d_v ones in each column. It means that every codeword bit participates in exactly d_c parity check equations and that every such check equation involves exactly d_v codeword bits. Low density parity check codes have been constructed mostly using regular random bipartite graphs. Here is an example of a regular parity check matrix with $d_c = 6$ and $d_v = 3$.

$$H = \begin{bmatrix} 1 & 1 & 1 & 0 & 0 & 1 & 1 & 0 & 0 & 0 & 1 & 0 \\ 1 & 1 & 1 & 1 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & 0 & 0 & 1 & 1 & 1 & 0 & 1 & 1 & 1 \\ 1 & 0 & 0 & 1 & 0 & 0 & 0 & 1 & 1 & 1 & 0 & 1 \\ 0 & 1 & 0 & 1 & 1 & 0 & 1 & 1 & 1 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 1 & 1 & 0 & 0 & 1 & 1 & 1 & 0 \end{bmatrix}$$

A graph associated with a parity check matrix A is called the Tanner graph and it contains two sets of nodes. The first set consists of N nodes which represent the N bits of a codeword; nodes in this set are called “bit” nodes. The second set consists of M nodes, called “check” nodes representing the parity constraints. The graph has an edge between the n th bit node and the m -th check node if and only if n th bit is involved in the m th check, that is, if $A_{mn} = 1$. Thus the Tanner graph is a graphical depiction of the parity check matrix. The bipartite graph corresponding to this parity check matrix is shown in Fig. 2.

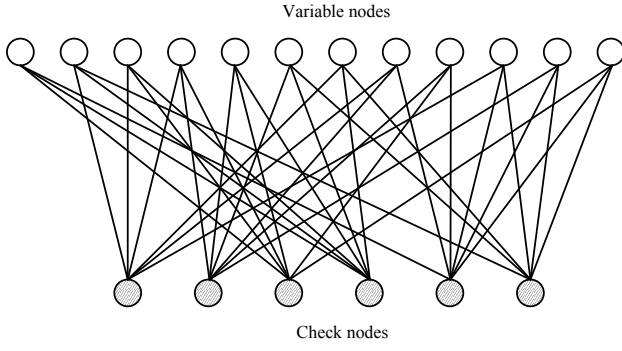


Figure 2. Bipartite graph corresponding to a regular parity check matrix

Let C be a regular LDPC code of length N and dimension K whose parity-check matrix A with $M = N - K$ rows and N columns contains exactly d_v 1's in each column (column weight) and exactly d_c 1's in each row (row weight). A_{mn} is the value of the m 'th row and n 'th column in A . The set of bits that participate in check is denoted: $N_m = \{n: A_{mn} = 1\}$. The set of checks that participate in bits $M_n = \{m: A_{mn} = 1\}$.

$$M_n = \{m: A_{mn} = 1\}$$

Assume codeword, $c = [c_1, c_2, c_3, \dots, c_N]^T$

Before transmission it is mapped to a signal constellation to obtain the vector, $t = [t_1, t_2, t_3, \dots, t_N]^T$

where

$$t_n = 2 * c_n - 1$$

which is transmitted through an AWGN channel with variance

$$\sigma^2 = N_0/2$$

$$r = [r_1, r_2, r_3, \dots, r_N]^T$$

Where

$$r_n = t_n + v_n$$

Here v_n is the Additive White Gaussian Noise (AWGN) with zero mean. Let hard decision vector

$$z = [z_1, z_2, z_3, \dots, z_N]^T$$

be

$$z_n = \text{sgn}(r_n)$$

$$\text{where } \text{sgn}(r_n) = \begin{cases} 1 & r_n > 0 \\ 0 & \text{otherwise} \end{cases}$$

The following notations concern bipartite graphs and message-passing algorithms running on these graphs, and will be used throughout the paper.

L_n : A priori information of bit node, n

$\bar{L}_n$: A posteriori information of bit node, n

$E_{m,n}$: The check to bit message from m to

$F_{n,m}$: The bit to check message from n to m

A. Sum Product Algorithm

The Sum Product Algorithm [17] can be summarized in the following four steps.

Step 1:

Initialization:-

A priori information, $L_n = -\infty$

Bit to check message initialization, $F_{n,m} = L_n$

Step 2:

Horizontal Step:-

Check node Processing:

$$E_{m,n} = \log \frac{1 + \prod_{n' \in N(m) \setminus n} \tanh(F_{n',m}/2)}{1 - \prod_{n' \in N(m) \setminus n} \tanh(F_{n',m}/2)}$$

Step 3:

Vertical Step:-

A posteriori information:

$$\bar{L}_n = L_n + \sum_{m \in M(n)} E_{m,n}$$

Bit node Processing:

$$F_{n,m} = \bar{L}_n + \sum_{m' \in M(n) \setminus m} E_{m',n}$$

Step 4:

Decoding Attempt:-

If $\bar{L}_n > 0$, $\bar{c}_n = 0$, else $\bar{c}_n = 1$

If $A\bar{c}_n = 0$ then the algorithm stops and $\bar{c}_n$ is considered as a valid decoding result.

Otherwise, it goes to next iteration until number of iteration reaches its maximum limit.

B. Log Likelihood Decoding Algorithm for Binary LDPC codes

Input: A , the received vector r , the maximum no. of iterations L , and the channel reliability L_c .

Initialization: Set $\eta_{m,n}^{[0]} = 0$ for all (m, n) with $A(m, n) = 1$.

Set $\lambda_{mn} = L_c r_n$

Set the loop counter $l = 1$.

Check node update: For each (m, n) with $A(m, n) = 1$, Compute

$$\eta_{m,n} = 2 \tanh^{-1} \left(\prod_{j \in \mathcal{N}_{m,n}} \tanh \left(\frac{\lambda_{mj}}{2} \right) \right)$$

Bit node update: For each (m, n) with $A(m, n) = 1$, Compute

$$\lambda_{mn} = L_c r_n + \sum_{m \in \mathcal{M}_{n,m}} \eta_{m,n}$$

Log pseudo posterior probabilities:

For $n = 1, 2, \dots, N$ Compute

$$\lambda_n = L_c r_n + \sum_{m \in \mathcal{M}_n} \eta_{m,n}$$

Make a tentative decision: Set $\hat{c}_n = 1$ if $\lambda_n > 0$, else set $\hat{c}_n = 0$.

If $A \hat{c}_n = 0$ then stop. Otherwise if no. of iteration < maximum no. of iteration, loop to check node update. Otherwise, declare decoding failure and stop.

C. Min Sum Decoding

The sum-product algorithm can be modified to reduce the implementation complexity of the decoder. This can be done by altering the Horizontal step:

$$E_{m,n} = \log \frac{1 + \prod_{n' \in \mathcal{N}(m) \setminus n} \tanh \left(\frac{F_{n',m}}{2} \right)}{1 - \prod_{n' \in \mathcal{N}(m) \setminus n} \tanh \left(\frac{F_{n',m}}{2} \right)} \quad (1)$$

using the relationship:

$$2 \tanh^{-1} p = \log \frac{1+p}{1-p}$$

Equation (1) can be rewritten as,

$$E_{m,n} = 2 \tanh^{-1} \prod_{n' \in \mathcal{N}(m) \setminus n} \tanh \left(\frac{F_{n',m}}{2} \right) \quad (2)$$

Equation (2) can be further modified as,

$$E_{m,n} = 2 \tanh^{-1} \prod_{n' \in \mathcal{N}(m) \setminus n} \operatorname{sgn}(F_{n',m}) \prod_{n' \in \mathcal{N}(m) \setminus n} \tanh \left(\frac{|F_{n',m}|}{2} \right)$$

$$= \prod_{n' \in \mathcal{N}(m) \setminus n} \operatorname{sgn}(F_{n',m}) 2 \tanh^{-1} \prod_{n' \in \mathcal{N}(m) \setminus n} \tanh \left(\frac{|F_{n',m}|}{2} \right) \quad (3)$$

the Min-sum algorithm simplifies the calculation of (3) even further by recognizing that the term corresponding to the smallest $F_{n',m}$ dominates the product term and so the product can be approximated by a minimum:

$$E_{m,n} = \prod_{n' \in \mathcal{N}(m) \setminus n} \operatorname{sgn}(F_{n',m}) \min_{n' \in \mathcal{N}(m) \setminus n} |F_{n',m}|$$

D. Normalized Min Sum Decoding

Normalized Min sum algorithm [16] further modifies the min sum algorithm by multiplying a normalizing factor (say v) where $0 < v \leq 1$ in the horizontal step.

$$E_{m,n} = v \prod_{n' \in \mathcal{N}(m) \setminus n} \operatorname{sgn}(F_{n',m}) \min_{n' \in \mathcal{N}(m) \setminus n} |F_{n',m}|$$

III. PROPOSED OPTIMIZED MIN-SUM ALGORITHM

1) Motivation

The foundation of our work is based on the improvement in performance of normalized min sum algorithm [16]. From descriptions in previous sections we have seen that the sum product decoding [7] has been reduced to different forms to reduce the complexity and through some compromise in performance. Min sum decoding [12] is one of them. Different works have been done on min sum decoding to improve its performance to get closer to sum product performance like normalized min sum decoding[16], adaptive min sum decoding[14], self corrected min sum decoding[15] etc. In these papers they proposed different factors which modifies and improves the performance in different ways. In the normalized min-sum algorithm a normalizing factor was proposed to be multiplied in check node. But the performance using normalized min-sum is far from the sum product decoding algorithm.

2) Optimization Factor, α

The main feature of our proposed algorithm is the use of the optimization factor. Multiplication of α both in check node and bit node update is the basic difference between this algorithm and Normalized Min-sum algorithm. In the

Normalized Min-sum algorithm, normalizing factor was only used for check node update [16]. We are also reducing the complexity of determining two different factors for check and bit node updates by using the same factor for both the updates. The value of optimization factor α varies for different Signal to Noise Ratio (SNR). For a particular SNR we took the value of α that causes the minimum Bit Error Rate (BER).

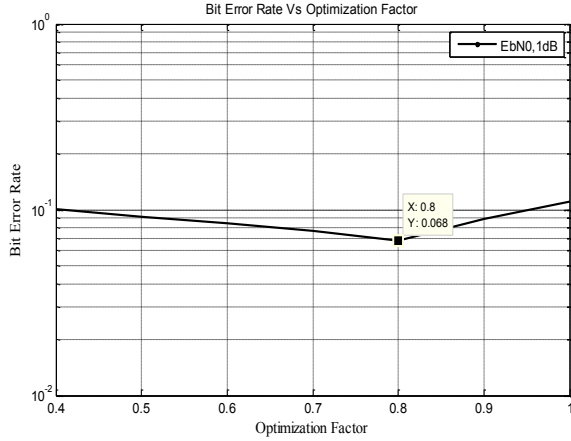


Figure 3. The impact of the optimization factor in the Optimized Min-Sum algorithm on the BER for the (2000, 1000) LDPC codes

Fig. 3 shows the variation of BER with respect to optimization factor, α for 1dB Signal to Noise Ratio. Here $\alpha = 0.8$ is selected for which the BER is minimum. This same procedure is followed to calculate α for different SNRs.

3) Proposed Algorithm

Already the normalized min-sum algorithm is explained. Therefore we state only the summary of our algorithm.

α : The optimization factor , $0 < \alpha \leq 1$

Iterative processing

Step 1: Initialization:-

A priori information, $L_n = -r_n$

Bit to check message initialization, $F_{n,m} = L_n$

Step 2: Horizontal step:-

Check node processing:

$$E_{m,n} = \alpha \prod_{n' \in N(m) \setminus n} \text{sgn}(F_{n',m}) \min_{n' \in N(m) \setminus n} |F_{n',m}|$$

Step 3: Vertical step:-

A posteriori information:

$$\bar{L}_n = L_n + \sum_{m \in M(n)} E_{m,n}$$

Bit node processing:

$$F_{n,m} = \bar{L}_n - \alpha E_{m,n}$$

Step 4: Decoding Attempt:-

If $\bar{L}_n > 0$, $\bar{c}_n = 0$, else $\bar{c}_n = 1$

If $A\bar{c}_n = 0$ then the algorithm stops and $\bar{c}_n$ is considered as a valid decoding result. Otherwise, it goes to next iteration until number of iteration reaches its maximum limit. The flow chart for this algorithm is shown below.

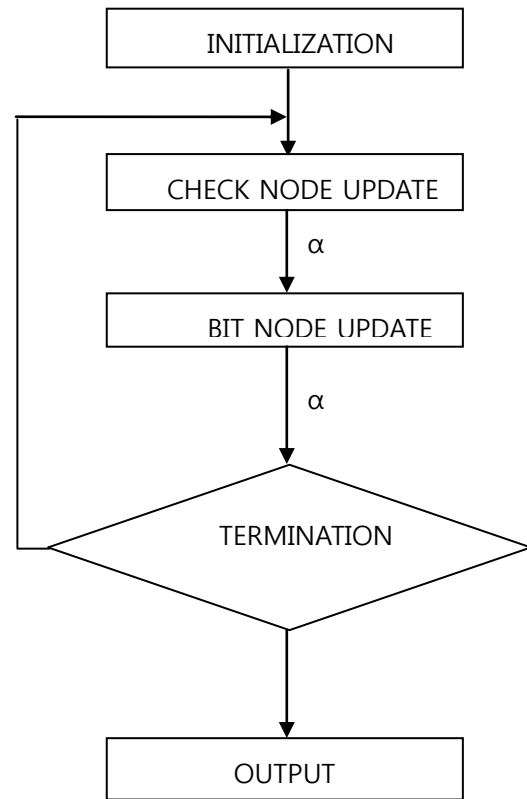


Figure 4. Flow chart of Optimized Min-Sum Algorithm

IV. SIMULATION

Regular (2000, 1000) [2] LDPC codes with code rate 1/2, row weight 3 and column weight 6 are used in our simulation. The codes are transmitted on AWGN channel after BPSK modulation. We set the maximum number of iteration to 50. The comparison among Sum Product (SP) [7], Min-sum (MS) [12], Normalized Min-sum (NMS) [16] and proposed Optimized Min-Sum (OMS) algorithms are shown in the Fig. 5. Simulation results show that the Optimized Min-sum obtains much better performance than MS, comparatively better performance than NMS and closer to that of Sum Product. Fig. 5 shows that for the BER value 10^{-2} , our algorithm can achieve 0.05dB decoding gain over NMS.

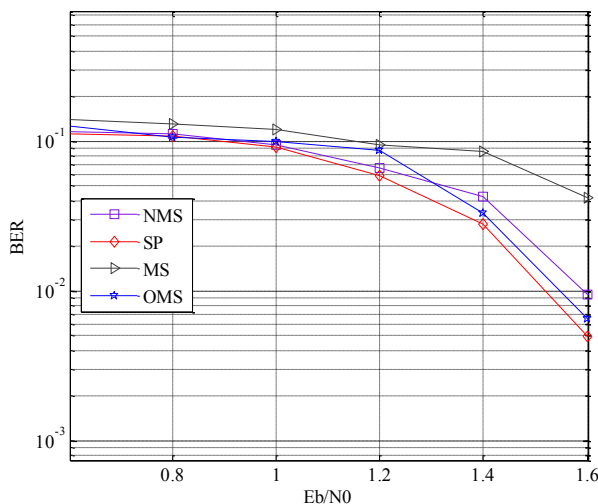


Figure 5. Bit Error Rate of LDPC codes (2000, 1000) for SP, MS, NMS, OMS

V. CONCLUSIONS

Through the introduction of Optimization factor we have obtained a better tradeoff between 'performance' and 'complexity'. We achieved much better performance than MS and NMS in exchange of slight increase in complexity. Using the same factor for both the nodes has reduced the complexity of calculating two different factors. And also the optimization factor is determined before the decoding process which causes no additional complexity in the decoding algorithm. Thus the proposed algorithm is a very competitive decoding technique for regular LDPC codes. Further analysis can be done for irregular LDPC codes.

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