## **Evolving Bio Plausible Design With Heterogeneous Noc**

Nithya Narayanamurthy\*, J. K. Periasamy \* \*Department of Computer Science & Engineering, Sri Sairam Engineering College ,Tamil Nadu, India <u>nithya.murthi@gmail.com</u>, jkperiasamy@gmail.com

*Abstract*— With the increasing complexity of various communication and multimedia standards, Network on Chip (NoC) is evolving as a solution for on-chip communication problems. Bio-inspired paradigms such as spiking neural networks (SNNs), when incorporated can take full advantage of their inherent parallelism and offer the potential to meet the demands of real-time fault tolerant applications. This paper presents a scalable, configurable 2-D irregular mesh network on chip (NoC)-based SNN architecture. The modules are placed in such a way to minimize the spatial traffic density, unnecessary switch links and nodes resulting in reduced SNN area requirements. The proposed design is based on a planar grid of switches that route the traffic according to a fixed shortest path (XYDT based) discipline. It uses input buffering scheme and employs multi-class wormhole forwarding to support multiple service priority classes thus ensuring QoS.



Nithya Narayanamurthy (M'12) : This author became a Member (M) of IEEE in 2012. She is pursuing her Bachelor of Engineering in Computer Science and Engineering at Sri Sairam Engineering College, affiliated to Anna University(India).



**J.K. Periasamy :** This author has completed his Master of Engineering and currently working as a Professor in the Department of Computer Science at Sri Sairam Engineering College, affiliated to Anna University(India).