Bit Error Rate Analysis for V-BLAST/STBC using Interference Cancellation Techniques

Chirawat Kotchasarn

Department of Electronics and Telecommunications Engineering, Rajamangala University of Technology Thanyaburi, Pathumthnani, Thailand, 12110 Tel: (662) 549-4620 Fax: (662) 549-4622 E-mail: chirawat.k@en.rmutt.ac.th

Abstract— Multiple Input Multiple Output (MIMO) systems have been extensively studied in context of wireless communication systems, which promising the both increased capacity and link level reliability. In this paper, we proposed the interference cancellation techniques for V-BLAST/STBC architecture, which integrates Alamouti space-time block code (STBC) layer together with vertical Bell-laboratories (V-BLAST) layer. In this work, we employ four transmit and three receive antennas over frequency flat Rayleigh fading channel. This paper presents signal detectors for V-BLAST/STBC with minimum mean square error (MMSE), zero forcing (ZF), parallel interference cancellation (PIC) and successive interference cancellation and the computational complexity of the joint optimal detection is better than the other detection technique.

Keyword— interference cancellation; Vertical Bell Laboratories Layered Space-Time; Space Time Block Code; zero forcing; minimum mean square error; successive interference cancellation; parallel interference cancellation



Chirawat Kotchasarn received the B. Eng. in electronics engineering from KMITL in 1996 and the M. Eng. in electrical engineering from KMUTT in 1999. He also received the Ph.D. in telecommunications from Asian Institute of Technology, Thailand in 2008. Currently, he is an assistant Professor at the department of electronics and telecommunications engineering RMUTT, Thailand. His main research areas are digital communications, mobile communications and signal processing in communications.