Sampling Jitter Mitigation with a Cascade Multiplier for Direct RF Bandpass Sampling Receiver

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***Abstract*—The sampling jitter is one of the main problems in the direct RF bandpass sampling receiver architecture. Sampling jitter will seriously degrade the performance of the receiver, which can be improved effectively by digital compensation algorithm. This paper investigates the sampling jittering mitigation for the direct RF bandpass sampling receiver. Under the direct RF bandpass sampling receiver architecture, an approximate sampling jitter model is derived. From the model, it is noted that the adverse impact of the sampling jitter is presented as the phase noise component of the carrier. As a result, a sampling jitter migration approach is developed to eliminate the phase noise. Specifically, the cascade multipliers is able to effectively migrate the sampling jitter. The proposed jitter mitigation method requires low complexity, and can be easily implemented by hardware. Moreover, it has many merits over the existing sampling jitter migration algorithms, including real-time sampling clock jitter elimination, flexible implementation to meet the specific performance requirements by selecting different level of cascaded sampling jitter migration structure. Several experiments have been conducted with 3GPP LTE type signals. The root-mean-square (RMS) and SNR are taken as the performance measurements. Experimental results show that the proposed sampling jitter migration method is able to remove the adverse effect of the sampling jitter with a comparable performance of existing techniques at much lower complexity.**

***Keyword*—direct RF bandpass sampling, sampling jitter, jitter mitigation, phase noise, cascade multiplier**

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