A High-efficiency HEVC Entropy Decoding Hardware Architecture

Hao Sun*, Li Zhou*, Hongji Xu*, Tao Sun**, Yang Wang*

** School of Information Science and Engineering, Shandong University, No.27, South Shanda Road, Jinan 250100, China*

*** Shandong Provincial Key Laboratory of Network Based Intelligent Computing, University of Jinan, P.R. China*

sunhao1990@gmail.com, *zhou_li@sdu.edu.cn, Corresponding Author

***Abstract*—High Efficiency Video Coding (HEVC) is becoming more and more important in current consumer application platforms. Compared with H.264 standard, it can reach up to 8192x4320 resolutions at 120fps. To accelerate HEVC decoding processing, this paper presents an efficient hardware entropy decoding architecture, Entropy decoding includes Colomb and CABAC decoding. Hierarchy ring buffer is designed to storage input bit-stream; Stack based Quad-Tree decoding structure is proposed for bit-stream parsing. Since CABAC decoder is a well-known bottleneck of the decoding performance, a 5-stage pipelined CABAC decoding engine is designed to accelerate the serial decoding progress. The proposed entropy decoding hardware architecture is verified on Altera Stratix IV FPGA running at a 200MHz clock frequency, using 8404 slices, memory size is 204KB.**

***Keyword*—HEVC, entropy, CABAC, architecture.**

Hao Sun, he was born on June 29, 1990. He received the BEng degree in Integrated Circuit Design and Integrated System from Shandong University, China, in 2013, and now he is pursing the MEng degree in Engineering of Integrating Curcuit in Shandong University. His current research interests include VLSI design and HEVC codec, etc

Li Zhou, she received doctor degree on 2004 from Zhejiang University, China. On 2004, Dr.Zhou joined Freescale semiconductor R&D center as principle design architect till 2009. As an architect and core team member, Dr.Zhou participated in multiple National high-tech SoC and HDTV fundamental research projects, led multiple 65nm/90nm 10 million gate scale VLSI SoC chips, and joined many VLSI project and architecture researches. From 2009, Dr.Zhou is an assistant professor in Shandong University, China. Her current research interests include stereo vision system algorithm and hardware design, GPU architecture and VLSI design, high performance processor architecture and VLSI design, etc.

Hongji Xu, received the B.S. degree in electronic engineering from Shandong University of Technology, Jinan, China, in 1999, and received the M.S. degree in signal and information processing and the Ph.D. degree in communication and information system from Shandong University, Jinan, China, in 2001 and 2005, respectively. He is currently an associate professor in the School of Information Science and Engineering at Shandong University. His research interests include wireless communications, ubiquitous computing, blind signal processing, and human-computer interaction.

Tao Sun, he received doctor degree on 2002 from Zhejiang University, China. Dr.Sun joined Suzhou China Core Co. Ltd as a researcher on CPU architecture and vice-general manager till 2007. From 2007 to 2009, Dr. Sun was a senior manager in Spansion China, led VLSI design projects. From 2009 till now, Dr.Sun is an associated professor in University of Jinan, China. His research interests include CPU/VLSI architecture, Solid storage architecture, etc.

Yang Wang, he was born on May 10, 1990. He received the BEng degree in Integrated Circuit Design and Integrated System from Shandong University, China, in 2013, and now he is pursing the MEng degree in Circuit and System in Shandong University. His current research interests include 3D-GPU and Computer Architecture etc.