A 1.8 V-to-2.5 V MIPI RFFE Slave Interface CMOS Circuit

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***Abstract*— The MIPI RFFE slave interface circuit including Power-on-Reset (PoR), SCLK receiver and SDATA bi-directional transceiver has been implemented with a CMOS 250 nm process. Simulation results show that the designed circuit has SDATA output transition time (for rise and fall) of shorter than 3.3 ns at a full-speed rate of 26 MHz, which satisfies the timing requirement (< 6.5 ns) by the specification of MIPI RFFE version 1.10. The target load capacitance that the designed MIPI RFFE slave interface circuit drives is 26 pF for the configuration of one master and eight slaves.**

***Keyword*— MIPI, RFFE, master, slave, PoR, SCLK, SDATA, CMOS, driver**

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