

# Inter-chip Wireless Interconnect System over PCB Medium Channels

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**Abstract**— A design scheme is proposed for wireless interconnection communication between chips. The PCB medium channel is built with absorber layer. Two chip pin antennas are designed and simulated. Their scattering parameters are extracted and compared with three different cases. It evaluates the bit error rate (BER) performance via a interconnect communication model with a coherent binary phase shift keying (BPSK) modulator and demodulator. Simulation results show that the designed system performance degrades with the increase of separation distance and signal noise ratio. A high data rate at 1 Gb/s with a low BER < 10<sup>-5</sup> can be achieved with the transmitted power of 10 dBm.

**Keyword**— Inter-chip, Chip Pin Antenna, Binary Phase Shift Keying, Absorber Layer, Bit Error Rate

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