Heterogeneous Reconfigurable Design for TreePM N-body Simulation

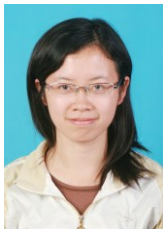
Linlin Zheng*, Xi Jin*, Bo Peng*, Tianqi Wang

**Department of Physics, University of Science and Technology of China, Hefei, Anhui Province, China*

linlinoo@mail.ustc.edu.cn, jinxi@ustc.edu.cn, pengball@mail.ustc.edu.cn, tqwang@mail.ustc.edu.cn

***Abstract*—In this paper, we describe our implementation for N-body simulation with the aid of FPGA, GPU and CPU. TreePM, which is a common algorithm for N-body simulation and meets our demands well, is chosen here. We split treePM algorithm into several parts, and assign them to different accelerators depending on the features of the operation. Moreover, partially dynamically reconfigurable FPGA architecture is used here for fine-grained scheduling, making the assignments more balanced. Experiments showed that it has improvement in speed and energy efficiency over previous design with the same scale. Besides, it's potential for advances with multiple clusters also been demonstrated here.**

***Keyword*—N-body, treePM, heterogeneous, partial configuration, FPGA**



Linlin Zheng received her B.S. degree from University of Science and Technology of China, and she is currently a M.S. student in Department of Physics in University of Science and Technology of China, Anhui, China, under the supervision of Prof. Xi Jin. Her current research work is mainly on FPGA-based Hardware Accelerator design.

Xi Jin received the B.S. degree from University of Science and Technology of China, Anhui, China, and he is currently an associate professor in Department of Physics in University of Science and Technology of China, Anhui, China. His research interests include SOC design technology, VLSI design, computer-aided design methodologies for SoC system integration and FPGA-based Hardware structure design.

Bo Peng received his B.S. degree and Ph.D. from University of Science and Technology of China, and he is currently a lecturer in Southwest University of Science and Technology. His current research work is mainly on FPGA-based Hardware Accelerator design and network.

Tianqi Wang received his B.S. degree from University of Science and Technology of China, and he is currently a Ph.D. student in Department of Physics in University of Science and Technology of China, Anhui, China, under the supervision of Prof. Xi Jin. His current research work is mainly on FPGA-based Hardware Accelerator and computing architecture.