Accelerating Eulerian Video Magnification Using FPGA

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***Abstract*—Video magnification can amplify and display the subtle motions that are impossible to see with our naked eyes. However, it's time consuming for CPU processing video magnification with high resolution. We propose a FPGA-based solution to Laplacian pyramid, temporal filter and pyramid reconstruction algorithm of the video magnification. The paper processes all pyramid levels and temporal filter with parallel and pipeline architecture. With the reconfigurable feature of FPGA, the temporal filter can be reconfigured which are all customizable by the user. We implement the whole video magnification system on Xilinx Kintex-7 FPGA board. When we process 1920 × 1080 video, the result shows that the hardware system is obviously speedup versus Eulerian Video Magnification on Intel i5 core.**

***Keyword*—Eulerian Video Magnification; FPGA; Laplacian pyramid; subtle motions; motion magnification**

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