Operating Frequency Improvement on FPGA Implementation of a Pipeline Large-FFT Processor
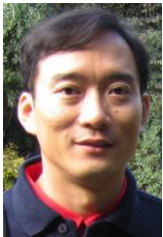
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Abstract— Requirement of large N-point FFT is found in niche areas such as astrophysics and radar applications. In recent years, there have been applications of large N-point FFT in consumer automotive radar, software-defined radio and ultra-wideband spectrum scanning, etc. The challenges are the processing speed and the cost involved. In this paper, circuit complexity reduction in FPGA implementation of large N-point Radix-22 Fast Fourier Transform (FFT) with single-path delay feedback architecture is reported. Memory requirement of the FFT in the FPGA consists of two parts, the RAM data storage of the feedback in each stage of the data flow and the twiddle factors prepared as ROM for each complex multiplication. Through address rearrangement, the ROM sizes for the twiddle factors are significantly reduced with the removal of redundancy. The reduction ratio is about $1/3(\log 4N-1)$. In the FPGA implementation, special control logic is introduced to cope with the uneven data flow pipeline caused by the outputs of the feedback registers and the twiddle factor multiplications. The operation processes of the FFT are designed and spread among the clock cycles. As a result, the signal critical path is reduced and the system clock frequency is increased. The proposed architecture is validated by the implementations of 1K and 4K Radix-22 FFTs in an Altera Cyclone IV FPGA, EP4CGX22, which is the second lowest capacity FPGA of the low cost series. For the 1K- and 4K-point FFTs, the operating frequencies are 231.11 MHz and 215.75 MHz, respectively, approaching 250 MHz which is the speed limit of the I/O ports of the FPGA.

Keyword— Fast Fourier Transform, FPGA

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