An Area-Efficient Multimode FFT Circuit for IEEE 802.11 ax WLAN Devices

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Abstract— Multi-mode fast Fourier Transform (FFT) circuits are essential in orthogonal frequency domain (OFDM) based systems which supports multiple bandwidth. Typically, hardware implementation employs a single FFT circuit for the highest supported bandwidth and using oversampling, the same FFT circuit is used to support lower bandwidth. For the new 802.11ax wireless local area network (WLAN) standard whose frame consists of the regular 3.2us length symbol as well as a longer 12.8us symbol, a fast switchable double-mode FFT circuit is required. In addition, the 802.11ax SIG-B symbol contains a maximum of two independent symbol streams that requires two FFT circuits for the 3.2us symbol length. Our proposed FFT architecture is optimized to support the 802.11ax standard with low latency, area and power requirements. FPGA implementation results show that our proposed circuit has efficiency 13.7% lower area compared to conventional architecture.

Keyword— OFDMA, IFFT/FFT, parallel FFT, SDF, MDC, 802.11ax.

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