Efficient FPGA Architecture for DPDK Flow Rules Processing

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***Abstract*—With the development of the Internet, the number of connected devices and the amount of transferred data increase annually leading to more complex network applications and limitations in data processing speed. The Data Plane Development Kit (DPDK) addresses these challenges by optimizing packet processing for high-speed network applications, including offloading processing tasks to Network Interface Cards (NICs) hardware using the rte_flow interface, which allows configuration of NICs offloads with specific flow rules. However, with the increasing complexity of network applications, the number of rules used is also growing rapidly, and more complexity. This presents a challenge for building and developing network systems capable of efficiently handling a large number of rules. This paper presents an architecture for processing the rte_flow interface using FPGA-based Smart NICs to leverage the reprogrammable capabilities of hardware accelerators. The architecture uses Ternary Content-Addressable Memory (TCAM) to reduce the key size in the rule tables, significantly increasing the number of rules and rule tables supported by the FPGA. Additionally, a custom DPDK driver (named VTL driver) is developed to manage and implement algorithms aimed at optimizing the number of rules in the hardware. To evaluate our proposed architecture, the Alveo U200 FPGA-based accelerator card is used to implement these features including 8 receive rule tables and 1 transmit rule table per ethernet port. Each table supports up to 2048 wildcard matches and 16384 exact match entries. The system achieves a network throughput of 100 Gbps per port and a rule insert rate of 204 million rules per second. These results significantly enhance hardware acceleration efficiency in networking.**

***Keyword*—** NIC, smartNICs, rte_flow, FPGA, DPDK, Offload, Wildcard match, Exact match, TCAM

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