GCCache: A Non-blocking and Low-latency General-purpose Context Cache Design for RDMA NICs

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***Abstract*—Remote Direct Memory Access (RDMA) network interface cards (RNICs) are widely used in AI large-scale model training and intelligent computing centers. However, current RNIC caches face several challenges, such as head-of-line (HOL) blocking, repeated processing of misses to the same memory address, high latency, and poor compatibility. To address these challenges, for the first time we propose GCCache: a non-blocking, low-latency, high-performance general-purpose cache architecture for RNICs. GCCache decouples hit processing and miss processing to enable non-blocking cache access and resolve HOL blocking. In addition, an outstanding request management mechanism ensures that for multiple misses to the same memory address, all corresponding requests are served immediately once the context is fetched, thereby saving PCIe bandwidth. Moreover, multi-request parallel processing and pipeline design reduce access latency and support context prefetching. GCCache supports all types of RDMA contexts (QPC, MPT, MTT, etc.) and multi-level page table queries. To the best of our knowledge, GCCache outperforms all currently published RDMA cache architectures in terms of latency and on-chip storage resources, with a cache processing latency of only 5 clock cycles and a throughput of 100 Gbps.**

***Keyword*—RDMA, cache architecture, FPGA.**

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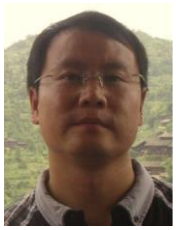

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